Service Manual

MP MASTER
MA33540

Send Section

PSS-19

for the frequency range 80 Hz to 25 MHz

BN 0871/00.83; Series A...

SEND SECTION PSS-19

for the frequency range 80 Hz to 25 MHz

Service Manual BN 871/01, Series A...

Order No. BN 0871/00.83
Edition 3121

1.9.84 Dav/sche
0.3.9.84

Subject to change without notice
Printed in the Federal Republic of Germany

Wandel & Goltermann

PRECISION ELECTRONIC
MEASURING INSTRUMENTS

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PRELIMINARY REMARKS, TEST EQUIPMENT

PRELIMINARY REMARKS

INTRODUCTION TO THE SERVICE PROCEDURE

Maintenance and repair are the two main tasks which occur when measuring equipment is serviced. The equipment handbook with its Operating Manual, its Service Manual, and the Appendix provides all necessary information.

The Operating Manual provides all necessary basic information on the instrument. Section 6 of this Manual describes non-electrical maintenance work such as cleaning and lubricating of moving parts wherever such work is necessary.

The Service Manual provides all specific repair information. Section 8 of this Manual "checking important specifications" is used for both maintenance and repair.

The information has been selected so that an experienced technician can execute all normal repair work. Tasks which normally occur only during manufacture of an instrument have been omitted.

The Appendix contains all block diagrams, circuit diagrams, parts lists and component layout diagrams of the printed circuit boards. In addition, it provides the necessary information for reading the circuit diagramsand ordering spare parts. It contains a German/English/French translation list for important terms used in the Appendix.

TEST EQUIPMENT

The test equipments listed here should be regarded as recommendations. Equivalent instruments made by other manufacturers can also be used.

Instrument	Requirements	Recommended Typ	Manufacturer	Used in Section
Level Generator	1 MHz to 100 MHz	PSS-14/BN 833/0	W & G	7.7.9,
Level Generator	10 kHz to 10 MHz	PS-19/BN 870/...	W & G	7.7.2, 8.5.2
Selective Level Meter	200 Hz to 180 kHz	SPM-11/BN 604	W & G	8.6.1
Selective Level Meter	25 MHz to 100 MHz	SPM-14/BN 830/0	W & G	7.7.9, 8.6.3
Selective Level Meter	10 kHz to 25 MHz	SPM-19/BN 829/...	W & G	7.7.6, 7.7.8, 8.3, 8.5, 8.6.2, 8.7
Milliwatt Power Meter with accessories	80 Hz to 25 MHz	EPM-1 BN 564/0	W & G	7.7.4, 7.7.5, 7.7.8 8.2, 8.4
Test Probe, 75 Ω		TK-10/BN 572/0	W & G	
Test Probe		TKS-10/BN 668	W & G	
Test Probe Adaptor		TKSA-124 BN 668/00.14	W & G	
Test Probe Adaptor		TKSA-150 BN 668/00.11	W & G	
Test Probe Adaptor		TKSA-600 BN 668/00.14	W & G	
Calibration Adaptor		TKSE-124 BN 668/00.24	W & G	
Calibration Adaptor		TKSE-150 BN 668/00.21	W & G	
Calibration Adaptor		TKSE-600 BN 668/00.22	W & G	
Universal counter	25 MHz	PM 6614/05	Philips	7.7.2
Digital voltmeter	4 1/2 digit	8600 A	Fluke	7.6.4, 7.6.5, 7.7.7 7.7.8, 8.3
Calibration Adaptor	75 Ω, 0 to 60 dB	D 2053	Siemens	8.3
Return Loss Measurement Attachment	124/150/600 Ω, 20 kHz to 1 MHz	RFZ-12 BN 810/01.00	W & G	8.5.2
Return Loss Measurement Bridge	75 Ω, 5 MHz	RFZ-14 BN 830/00.01	W & G	8.5.1
Oscilloscope	f > 150 MHz	475	Tektronix	7.7.2, 7.6.4
RF voltmeter	f > 1 MHz, 10 MΩ/25 pF	400 E	hp	7.6.4, 7.7.3
Logic Tester	TTL, CMOS	TKL-515	W & G	7.6.4
DC voltage source	0...5 V, Z_{out} < 200 Ω	6960 A	hp	7.6.4.5
Ω-meter		PANOHM	Gossen	7.1.1

Figure 1 Recommended test equipment

Designation	Type	Manufacturer	Used in Section
Attenuator, 40 dB	DG-940/BN 920/43	W & G	8.6.3
Terminating impedance 75 Ω, coax.			8.6.1
Terminating impedance 124 Ω, bal.			8.6.1
Terminating impedance 150 Ω, bal.			8.6.1
Matching pad 75 Ω/150 Ω			7.7.9

Figure 2 Other testing aids and special tools

INTRODUCTION TO THE SERVICE CONCEPT OF THE DIGITAL SECTION

The instrument software includes several test programs. Together with a few other test facilities in the PSS-19, these programs make it possible to check the complete digital section of the PSS-19 without further equipment and, under certain circumstances, to localize the fault[1)].
With microprocessor controls, faultfinding in normal operation is not normally expedient.

Test equipment for servicing the digital section

- Signature analyzer 5004 A hp
- Oscilloscope, limit frequency > 100 MHz
- Ohmmeter (e.g. TRI OHM, Gossen)

FAULTFINDING IN THE AGC AMPLIFIER

The aim of the faultfinding strategy shown in Section 7.6.4.5 is to detect and localize faults in the AGC amplifier and to determine whether the complete AGC amplifier must be replaced or whether it can be repaired.

Hints are given for possible repairs. These can be divided into two classes: repairs where components can be replaced without problems and repairs which require subsequent recalibration of the instrument.

1) The Service Manual only contains enough signatures to localise a fault to a single module.

7 TROUBLESHOOTING AND REPAIR INFORMATION

7.1 SAFETY PRECAUTIONS

7.1.1 PREVENTION OF ELECTRICAL ACCIDENTS

Safety class

This instrument belongs to safety class I in accordance with VDE 0411 or IEC Publ. 348. The enclosed mains cable contains a protective conductor. Except in specially certified rooms, the mains plug may be inserted only in mains outlet sockets with a ground contact. It is not permitted to disconnect the protective conductor either inside or outside the instrument.

Opening the instrument

If covers are opened, or parts removed with the aid of tools, components carrying voltages may be exposed. Connection terminals may also carry voltages.

Before opening the instrument, it must be disconnected from all voltage supplies.

If calibration, maintenance, or repair is subsequently necessary with the instrument open and connected to the supply voltage, then this may be carried out only by a trained person who is familiar with the accompanying risks.

Capacitors within the instrument may still be charged, even if the instrument has been disconnected from all voltage supplies; see the notes in the circuit diagrams.

Fuses

Only the prescribed fuses may be used.

Repair, replacement of parts

Repairs have to be carried out in a professional manner. Care must be taken that the design features of the instrument are not modified in a way that would reduce safety. In particular, the leakage and air gaps and the spacing provided by insulation must not be reduced.

Use only original parts for replacement. Other spare parts are permissible only if they do not reduce the safety of the instrument.

Checks after repair and maintenance

Checking the protective conductor

Correct connection and good condition is checked by visual inspection and by measuring the resistance between the protective conductor pin of the plug and the chassis of the instrument. This resistance should be $< 0.5\ \Omega$. Move the cable while measuring the resistance; variations in the resistance value indicate damage in the cable.

Checking the insulation resistance

Measure the insulation resistance at 500 V DC between the mains pins and the protective conductor pin. The mains switch of the instrument should be in the "on" position for this test. The insulation resistance should be $> 2\ M\Omega$.

7.1.2 HOW TO PREVENT CIRCUIT DAMAGE

Caution when handling MOS components!

Some of the components in this instrument are MOS (metal-oxide semiconductor) components. These are easily damaged by static charges, ripple voltages from ungrounded instruments, or other interference potentials. Destruction by static charges can be avoided by observing the following rules:

- MOS components should remain in their delivery package until required for use. All terminals must be connected together (in black, electrically-con ductive foam material) until the component is required.
- Before removing MOS components or printed circuit boards equipped with such components from their packing materials, the electrically-conductive part of the packing materials must be brought into contact with a conductive bench top or the chassis of the instrument to be repaired.
- Before touching MOS components, grasp the conductor acting as a reference potential with one hand.
- All tools, instruments, the instrument section being repaired, and the person carrying out the repairs should have the same potential as the conductor which acts as the reference potential (e.g. a conductive bench top or, alternatively, the chassis of the instrument being repaired). For this reason, tools with which MOS components are to be handled should first be brought into contact with this reference potential. The tools must not have insulated handles.
- If a printed circuit board or other part of the instrument is being handled separately from the instrument itself, and is not placed on a conductive bench top, then the ground of the printed circuit board or assembly must be connected to the reference potential.

Destruction due to ripple voltages during soldering can be avoided by establishing a permanent contact between the soldering iron and the chassis of the instrument being repaired.

MOS components can be identified by the letters MOS, CMOS or MOSFET in the component designation of the parts list.

7.2 SOLDERING INSTRUCTIONS

We recommend the use of thin solder with a small amount of flux. The following rules should be observed:

- Soldering times for all components $\leq$ 5 s;
- Soldering temperatures $\leq$ 260° C;
- Avoid getting drops of flux on switch contacts;
- When soldering on switch contacts or other electromechanical components, ensure that the flux cannot flow into the contact.

Hint for unsoldering multi-pin components

Extraction of the solder from each pin with the aid of special unsoldering tool is by far the best method. During unsoldering, move the component backwards and forwards to ensure that each pin is free. Do not use force: through-plated holes are easily damaged by pulling out pins which are not completely free! In the case of dual in-line components, damage to the printed circuit board can be avoided by cutting off the pins on the component side and then unsoldering each pin separately.

Soldering on thin film circuits

Soldering on thin film circuits requires precise temperature control, very short soldering times, and special aids. The danger of destroying the circuit with normal soldering methods is so high that we recommend that the complete thin film circuit be replaced.

7.3 INSTRUMENT IDENTIFICATION

The following instrument identification is necessary for inquiries, for ordering spare parts, or for checking whether this Service Manual belong to the instrument being repaired:

Type designation, designation of the special version,
installed options, series index, and serial number.

Figure 7-1 shows where this information can be found.

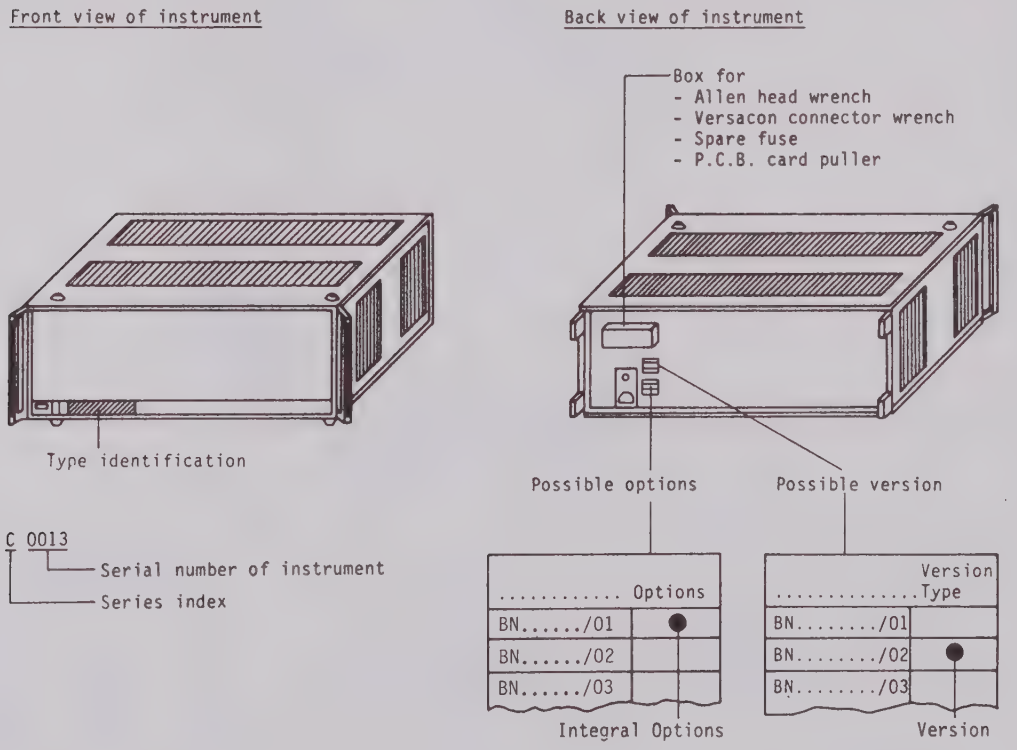


Figure 7-1 Instrument identification

7.4 TAKING THE INSTRUMENT APART

See Figure 7-2 for removal of the instrument

See Figure 7-3 for removal of the control knobs

See Figure 7-4 for screening cases and the frame

After removal of the 6 upper Allen head screws, the instrument is lifted upwards and out from the enclosure. The power supply remains in the enclosure. It is, however, connected to the instrument by a wiring harness.

Tool:
Allen wrench, Sw = 3
(see back panel)

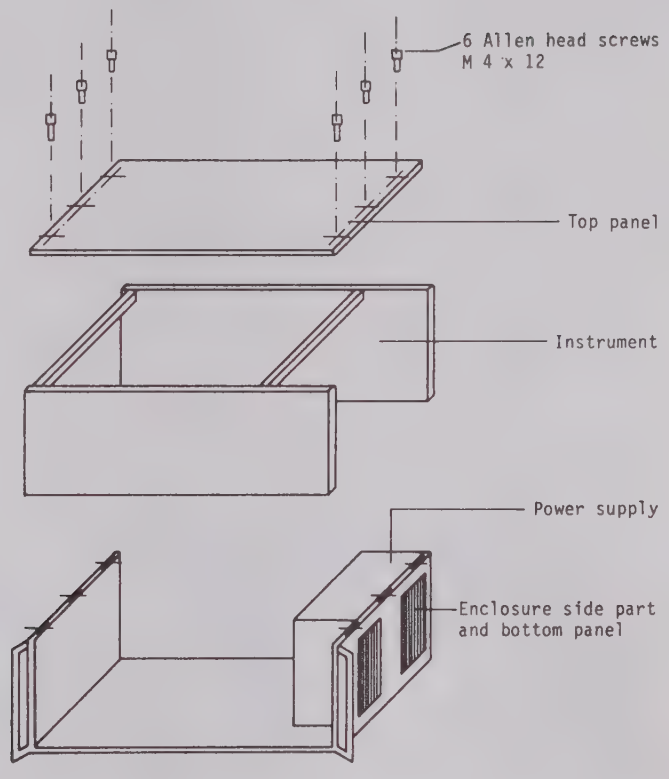
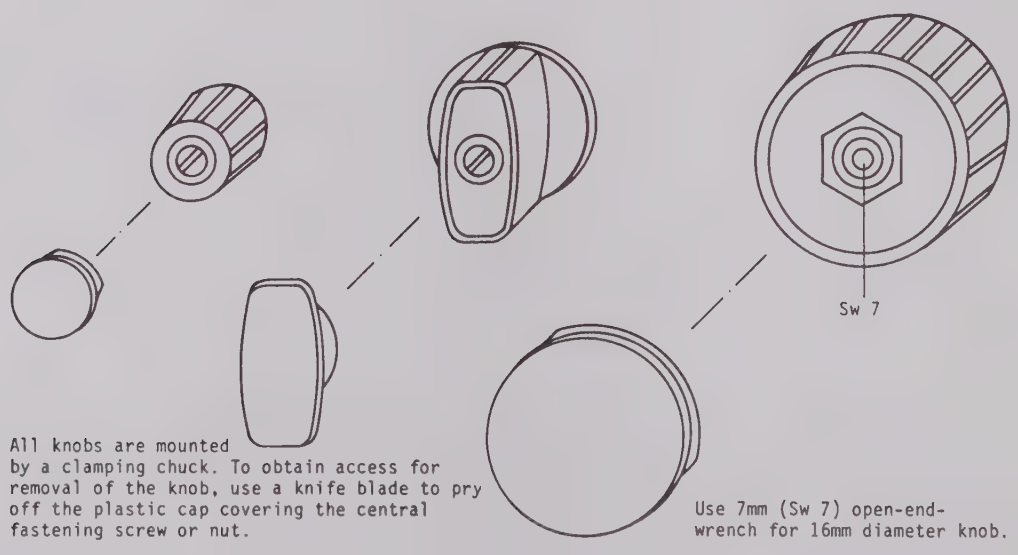


Figure 7-2 Removal of the instrument



All knobs are mounted by a clamping chuck. To obtain access for removal of the knob, use a knife blade to pry off the plastic cap covering the central fastening screw or nut.

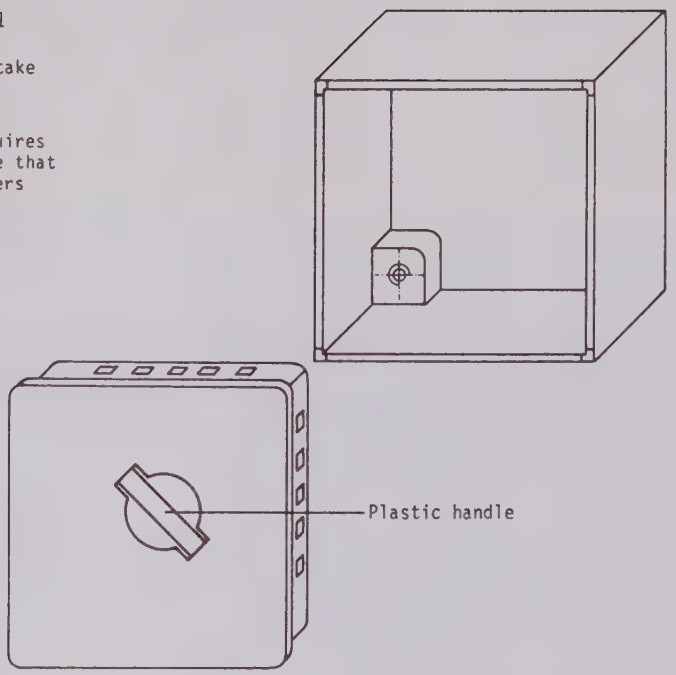
Use 7mm (Sw 7) open-end-wrench for 16mm diameter knob.

Figure 7-3 Removal of control knobs

Removal of cover from screening boxes and frames

The plastic handle is used to take the covers off from the frames and boxes.

Caution: replacing a cover requires attention to make sure that the thin contact fingers are not damaged.



Disassembly of circuits from screening boxes and frames

The stand-off screws or spacers to which the printed circuit board is attached, and all chassis-ground screws should be removed. Then the printed circuit board is removed by the card puller.When replacing the circuit the contact pins must be protected by assuring the p.c.b. is exactly parallel to all pins before the p.c.b. is pressed home.

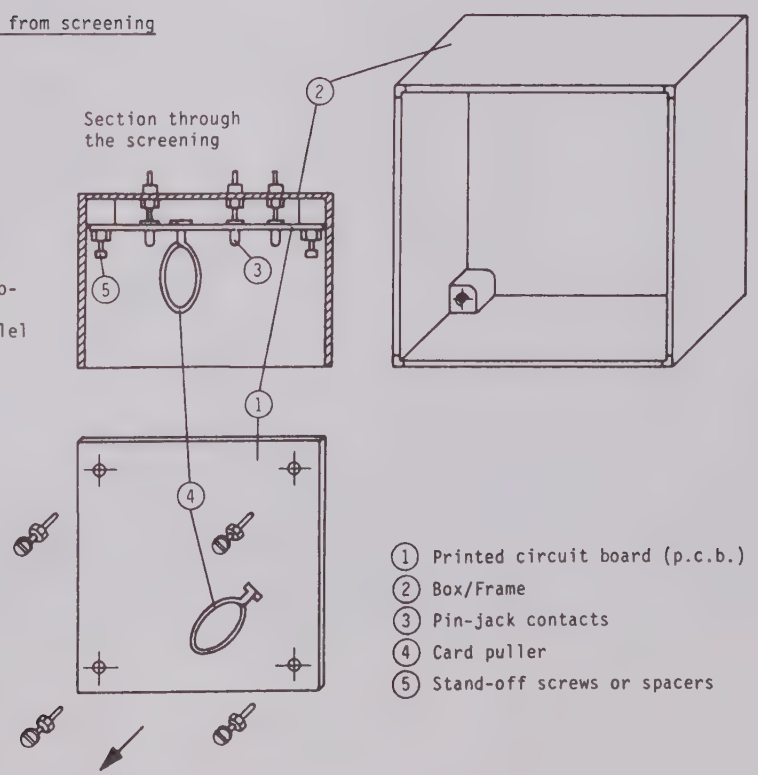


Figure 7-4 Screening cases and frames

7.5 POSITION OF ASSEMBLIES, ALIGNMENT COMPONENTS, TEST POINTS

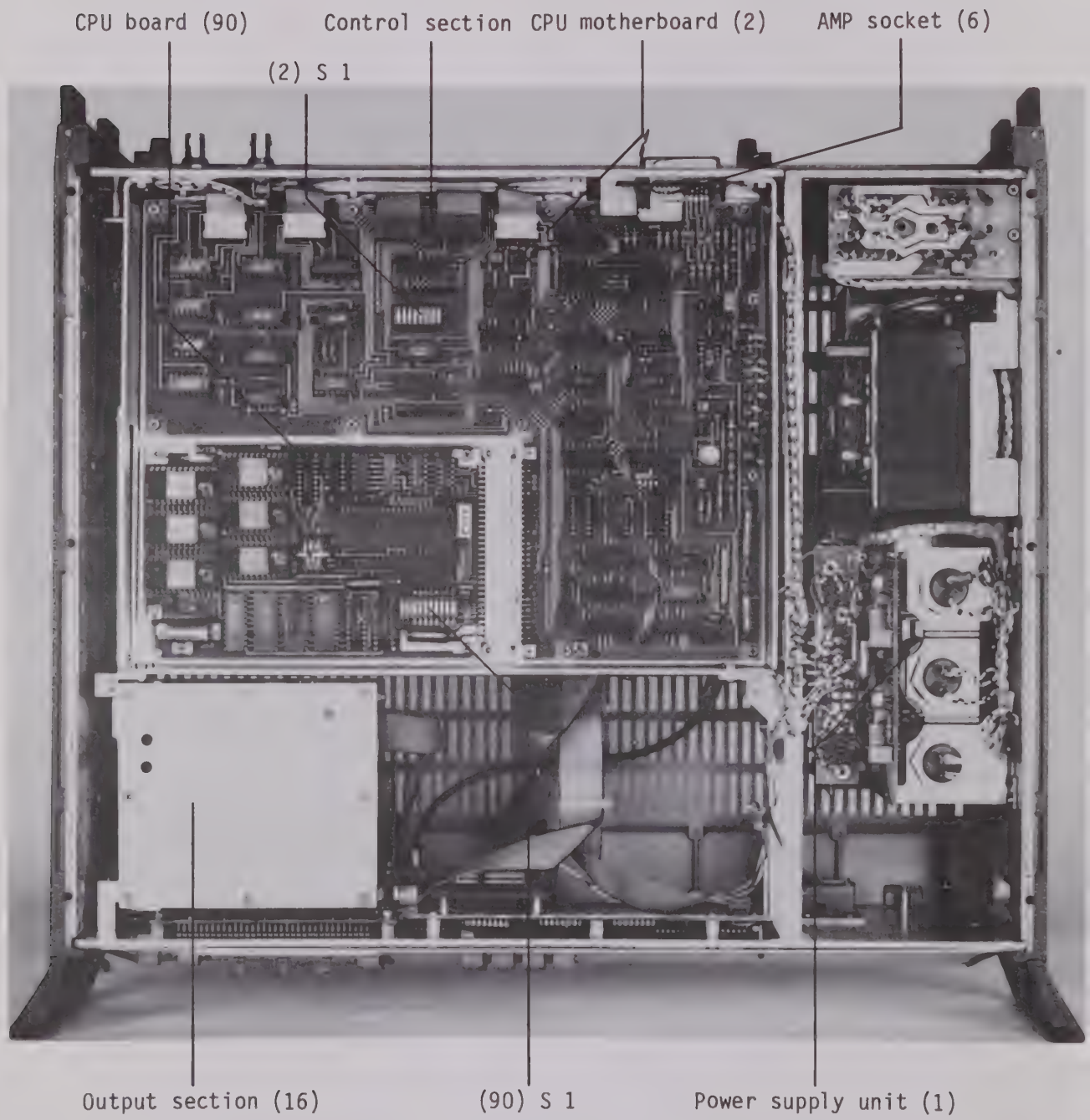


Figure 7-5 Top view of instrument

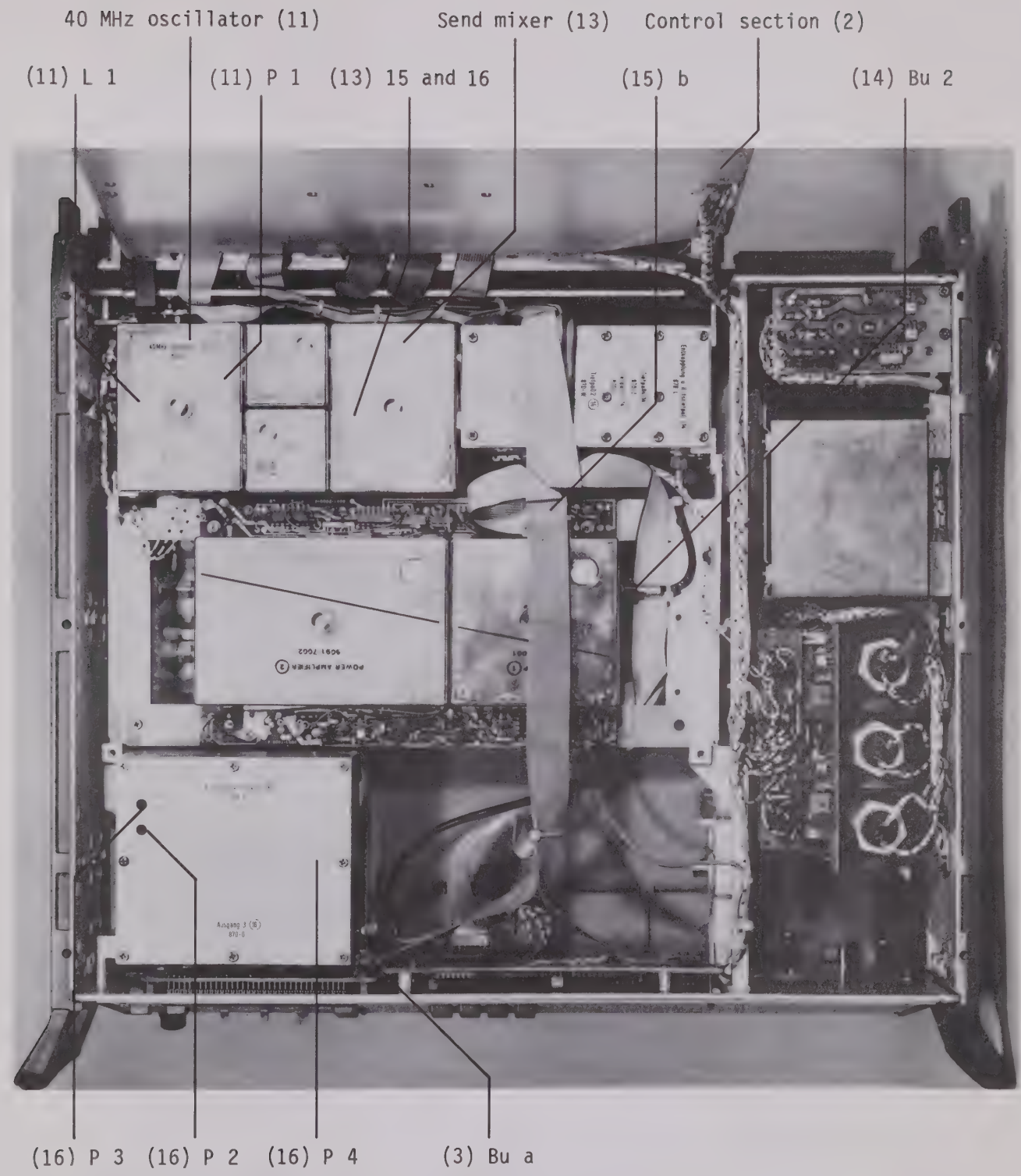


Figure 7-6 Top view of instrument with control section raised

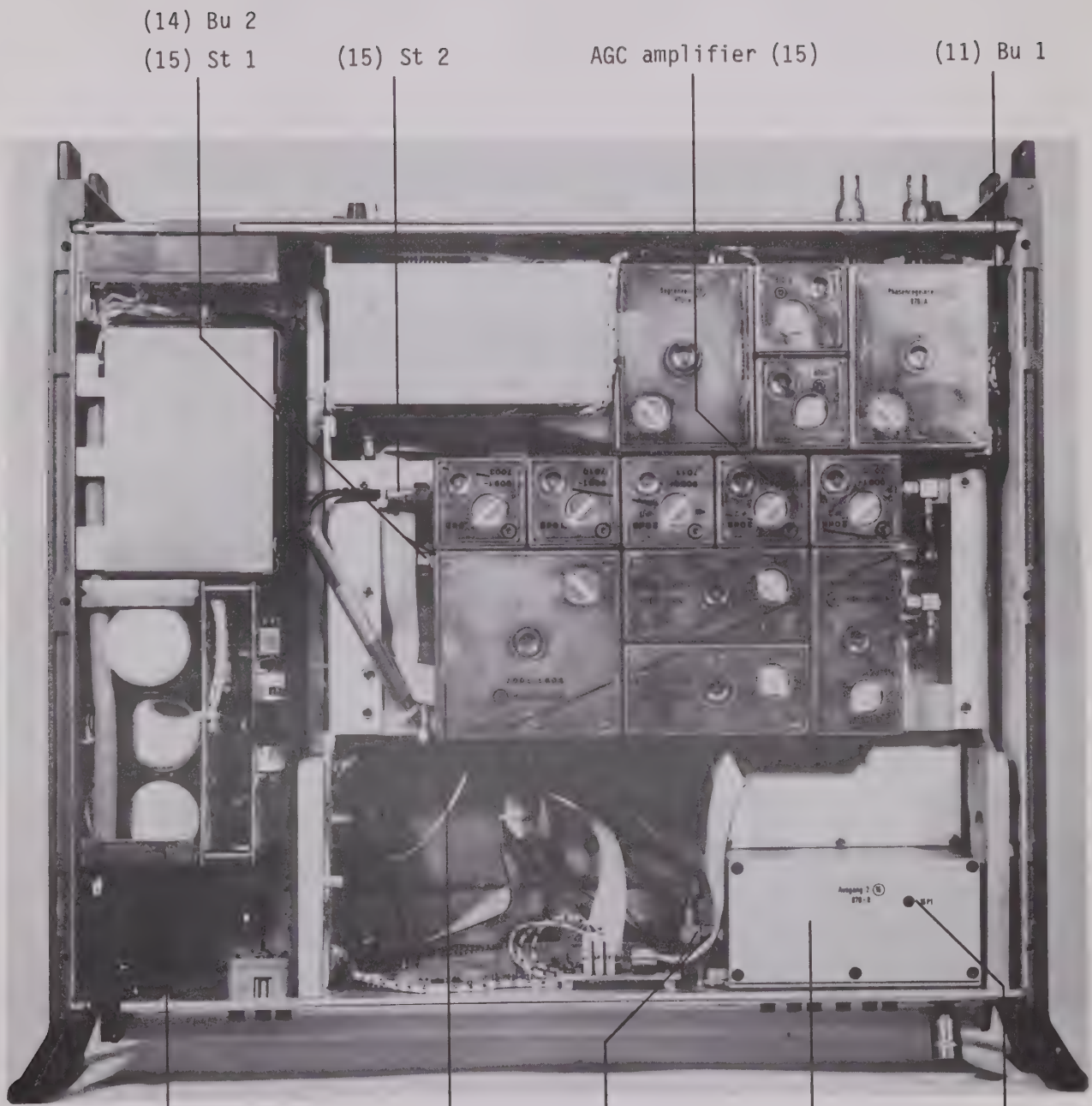


Figure 7-7 Bottom view of instrument

7.6 FAULTFINDING NOTES

7.6.1 INTRODUCTORY REMARKS ON THE NEW MEASURING AND TESTING METHODS

7.6.1.1 Signature analysis

With the aid of a signature analyzer (e.g. hp 5004A/5005A), digital signal sequences of any length can be checked uniquely and easily. Constant signatures (4-digit, pseudo-hexadecimal) are generated on the lines to be tested when defined and repeatable bit patterns exist with respect to a time window (START/STOP frame). The microprocessor is forced to generate such bit patterns by stimulus programs or external connections.

With the aid of a switch on the CPU board, the data lines AD0 ... AD7 are connected to +5 V, and line AD7 is also connected via a Schottky diode to the signal RD, thus generating the "processor free-running" signal. During the read operation, data lines AD0 to AD6 are HIGH and AD7 = RD = LOW. The free-running instruction is thus 7FH = MOV A,A. If the most significant address bit A15 is used as the time window = START/STOP frame, the processor increments through the complete address range from 0000 to FFFF. Each address line generates a unique signature. A signal which lies correctly within the timing condition, in the case of the µP 8085 the signal RD, is used as a CLOCK signal. The time relationships between the signals CLOCK, DATA, START, and STOP must always be correct, as unstable signatures will otherwise occur. Two frequently used signatures are explained briefly below:

The signature of the 0 V line is independent of the START/STOP frame and always 0000. The signature of the +5 V line is called the "CHARACTERISTIC SIGNATURE". This characteristic signature indicates whether the START/STOP frame is correctly connected and whether the edges of the START/STOP frame are correct. It also indicates that the µP is running.

If the characteristic signature occurs on an address or data line, then this indicates a short circuit to the supply voltage; if the signature 0000 occurs, the short circuit is to ground. If two address or data lines have the same signature, then there is probably a short circuit between these two lines. If the address range during free-running operation is restricted to the ROM addresses (START/STOP frame corresponds to the appropriate chip select signal), the data lines carry a bit stream which corresponds to the ROM contents.

In contrast to the ROM, where the data remain unchanged, the contents of the RAM and the I/O area depend on the current "status" of the instrument. In order to obtain useful signatures, specific information, which can be checked, must first be written into the RAM, and the I/O ports must be addressed periodically. These tasks can be fulfilled only by a program, which is called the stimulus program. Such programs can, for example, be called with the aid of a switch. When the instrument is switched on, the µP executes the initialization routine. During this, the switch position = bit pattern for calling specific stimuli is interrogated and the program is continued at the appropriate point.

7.6.2 FAULT LOCALIZATION PROCEDURE

The PSS-19 contains various programmed facilities as a faultfinding aid. When the instrument is switched on, an automatic RAM/ROM test is executed. After this, stimulus programs can be selected with a switch in order to test various sections of the instrument. The following structogram shows a possible sequence for faultfinding.

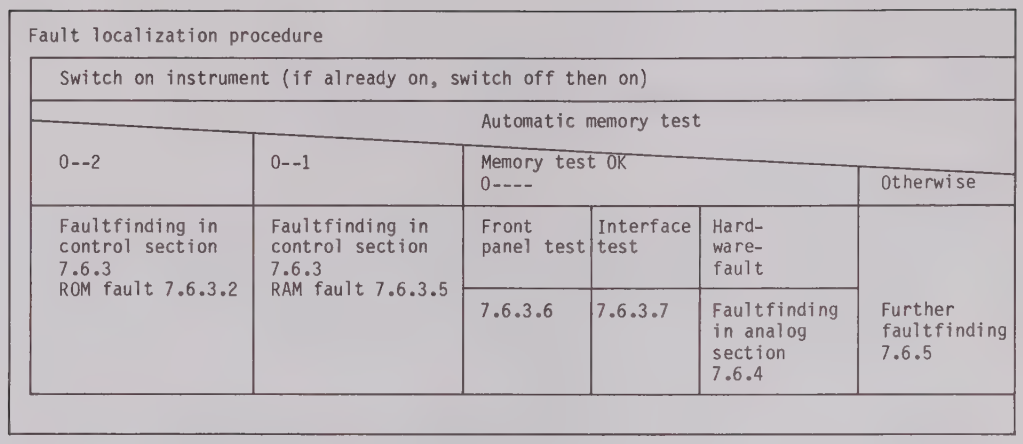


Figure 7-8 Concept of fault localization

7.6.3 FAULTFINDING IN THE CONTROL SECTION

7.6.3.1 Procedure

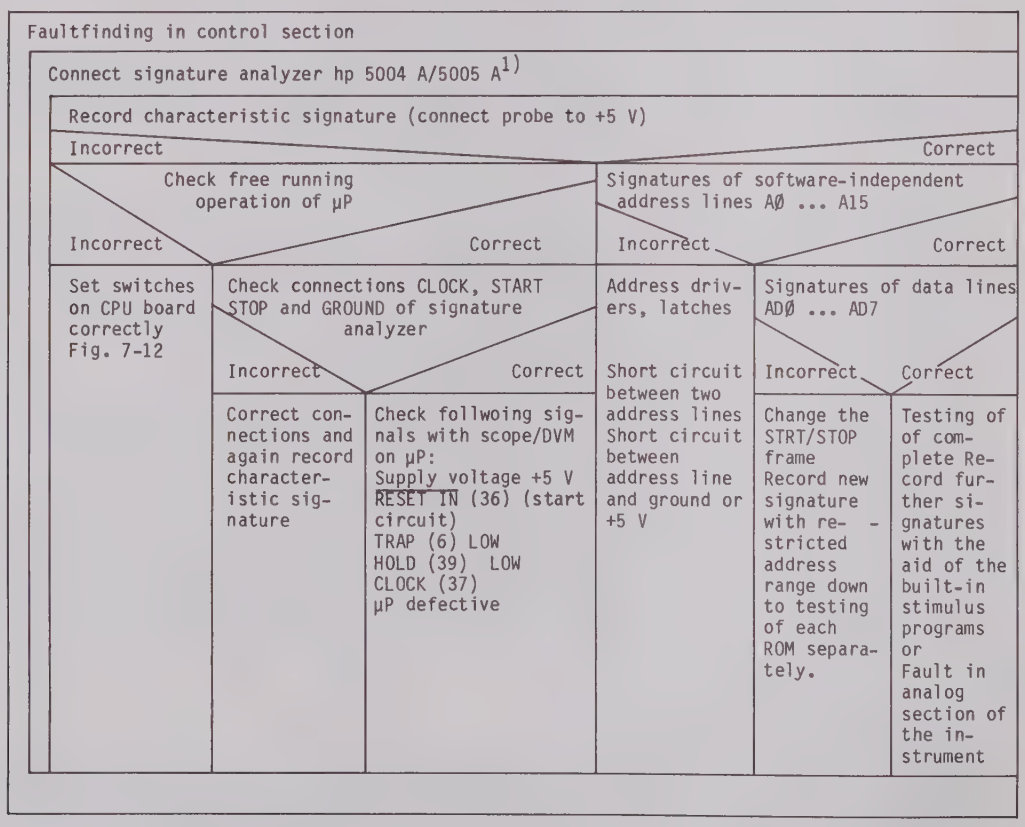

Faultfinding in control section
Connect signature analyzer hp 5004 A/5005 A1)
Record characteristic signature (connect probe to +5 V)
Incorrect
Correct
Check free running operation of µP
Incorrect
Correct
Signatures of software-independent address lines AØ ... A15
Incorrect
Correct
Set switches on CPU board correctly Fig. 7-12
Check connections CLOCK, START STOP and GROUND of signature analyzer
Incorrect
Correct
Address drivers, latches
Signatures of data lines ADØ ... AD7
Incorrect
Correct
Correct connections and again record characteristic signature
Check follwoing signals with scope/DVM on µP:
Supply voltage +5 V
RESET IN (36) (start circuit)
TRAP (6) LOW
HOLD (39) LOW
CLOCK (37)
µP defective
Short circuit between two address lines Short circuit between address line and ground or +5 V
Change the STRT/STOP frame Record new signature with re- - stricted address range down to testing of each ROM separately.
Testing of of complete Record further signatures with the aid of the built-in stimulus programs or Fault in analog section of the instrument

Figure 7-9 Faultfinding in the control section

1) Instruments made by other manufacturers will not necessarily display the same signatures

For the service programs, the following settings must be made on the instrument:

- Switch off the instrument
- Service switch S 1 on the CPU mother board

  Significance of switch

Switch	ON	OFF	Meaning
S 1.1		X	Z_{out} switching
S 1.2		X	Standard
S 1.3	X		Master reset
		X	Reestablish parameters which existed before power failure
S 1.4		X	Standard
S 1.5	X		Must be set to "ON" (in operation)
S 1.6			Any

Figure 7-10 Switch settings for servicing

Switch					Indication in level display	Test
1.1	1.2	1.3	1.4	1.5		
0	0	0	0	0	P--1	CPU-TK stimulus and I/O
1	1	1	0	0	P--2	Front panel test
1	0	1	1	0	P--4	Frontpanel stimulus

Figure 7-11 DIP switch on CPU motherboard

0 = switch open 1 = switch closed

Procedure for recording the signature:

Switch off the instrument

Set switch on CPU board to position TEST

	1	2	3	4	5	6	7	8	9	10
off	X	X	X	X	X	X	X	X	X	
on										X

Figure 7-12 DIP switch on the CPU board

7.6.3.2 Measuring the address signatures

Connection of the signature analyzer

GROUND to TP 1 on the CPU board

CLOCK to TP 6, edge ⎍

START/STOP to TP 2, edge ⎍

The processor steps through all addresses from ØØØØ to FFFF. The signatures specified below are valid for the complete address bus. For this reason, the signal names are specified rather than the IC PIN. The free-running switch must be set to the test position.

Characteristic signature ØØØ1	
Signal	Signature
A0, SA0	UUUU
A1, SA1	5555
A2, SA2	CCCC
A3, SA3	7F7F
A4, SA4	5H21
A5, SA5	OAFA
A6, SA6	UPFH
A7, SA7	52F8
A8, SA8	HC89
A9, SA9	2H70
A10, SA10	HPPO
A11, SA11	1293
A12, SA12	HAP7
A13, SA13	3C96
A14, SA14	3827
A15, SA15	755U

Characteristic signature ØØØ1	
Signal	Signature
$\overline{v0}$	5FU8
$\overline{v1}$	29A6
$\overline{v2}$	64HP
$\overline{v3}$	1181
$\overline{ROM0}$	3APF
$\overline{ROM1}$	02H7
$\overline{ROM2}$	2828
$\overline{ROM3}$	5P18
$\overline{ROM4}$	8P4P
$\overline{ROM5}$	9810
$\overline{ROM6}$	A277
$\overline{ROM7}$	A68C
$\overline{RAM0}$	3H1P *)
$\overline{RAM1}$	9C98 *)
$\overline{RAM2}$	7649 *)
$\overline{RAM3}$	24PC *)

Figure 7-13 Address signatures

7.6.3.3 Measuring the data signatures

Set the free-running switch (see 7.6.3.2)

Connection of the signature analyzer

	Connection	Edge
GROUND	TP 1 on CPU board	
CLOCK	TP 6 (RD) on CPU board	⌐

IC	ROM	Const. reg. No.	START	STOP
2	Ø	XXX.9311.XXX	TP 2 ⌐	TP 3 ⌐
3	1	XXX.9312.XXX	TP 2 ⌐	TP 3 ⌐
4	2	XXX.9313.XXX	TP 3 ⌐	TP 4 ⌐
5	3	XXX.9314.XXX	TP 4 ⌐	TP 4 ⌐
6	4	XXX.9315.XXX	TP 4 ⌐	TP 5 ⌐
7	5	XXX.9316.XXX	TP 5 ⌐	TP 5 ⌐

Figure 7-14 Measuring the ROM signatures

*) S 1.9 off

If the signatures of the ROMs are correct, it can be assumed that the ROM, the address bus and the drivers of the data bus (without the delay bus) are operating correctly. The data signatures can be extracted either directly from the EPROM or alongside the free-running switch.

The signature at PIN 18 of the ROM being measured is ØØØØ; for all other ROMs, it is the frame signature 7A7O.

7.6.3.4 Signature tables

EPROM/type 2716
The IC is programmed with the PROM PROGRAMMER Data I/O model 16. Before programming, the master EPROM must be checked. The erase window of the programmed IC must be covered with an adhesive label. The drawing No. for this adhesive label is provided in the parts list.

Const. reg. No.	Designation	Test code	Signatures (+5 V frame 7A 7O)								Instr. series
			D0	D1	D2	D3	D4	D5	D6	D7	
871-9311.008	90 IC 2	439D	28UU	3H84	4119	237A	2744	900F	P1P6	U12U	Only A
871-9311.011	90 IC 2	439D	OAAH	HAP5	777F	HCHF	2744	A669	P1P6	U12U	B...
871-9312.007	90 IC 3	234C	HOHH	545A	3U5H	5UC6	897F	5UHH	89UA	OU99	A...
871-9313.006	90 IC 4	E43B	93H1	6U51	A42P	PAHA	145F	0126	7414	UF71	Only A
871-9313.019	90 IC 4	E4C8	C5P2	9HF8	56C7	1843	145F	2715	7414	C017	B...
871-9314.005	90 IC 5	1C3E	A131	7379	9A29	4423	P222	19A3	A264	9908	A...
871-9315.004	90 IC 6	89AD	ACU1	3F49	61HO	5917	AA5O	3U33	2713	6H4P	Only A
871-9315.017	90 IC 6	155D	651A	P92P	HH8C	F585	PH7H	58UP	7820	AAF1	B...

Figure 7-15 EPROM signatures

7.6.3.5 RAM errors

It is not possible to check the RAM with the free-running signature. This instrument has RAMs only on the CPU board. A defect is automatically indicated by the error nummber O--100 after the instrument is switched on. In this case, we recommend that the CPU board be replaced.

Note: After recording the signatures, return the free-running switch to its normal operating position! S 1.1 to S 1.9 closed and S 1.10 open.

7.6.3.6 Front panel test

Carry out the following setting on CPU motherboard (2):

- Close 2 S 1/1 to 2 S 1/3
- Open 2 S 1/4 and 2 S 1/5
- Disconnect flat cable a
- Switch on instrument

The level display indicates "P--2"

Principle of the test:

For this test, all pushbuttons on the front panel are depressed in any sequence. Depression of a pushbutton is acknowledged clearly on the display in such a way that all display elements are tested. The indication remains displayed as long as the pushbutton is held down.

The following applies to all pushbuttons:

- The indication "P--2" disappears or is replaced by another indication as soon as the depression of the pushbutton is detected by the computer.
- All positions of the display are filled with "P" if the contact bounce suppression hardware cannot suppress contact bounce sufficiently. This display disappears after approximately 1 second.
- All positions of the display are set to "L" if an error is detected in the pushbutton matrix, for example, if a pushbutton cannot be clearly identified by the software.

Pushbuttons alongside or below an LED:

- The LED lights as long as the pushbutton is depressed.
- In the case of the pushbuttons dBm, dBm0, dBr, the unit also appears in the level display.
- In the case of the pushbutton dBm/dBm0, the diode "remote" lights and the unit dBm0 appears in the level display.

Toggle switches below the level display:

- The position of the depressed switch is indicated in the level display by "H". A switch which is not depressed is indicated by "-".
- The direction of the switch operation is simultaneously indicated by an arrow in the level display.

Toggle switches at the bottom of the front panel:

- Each time the switch is depressed, the light in the row of indicators to the left of the switch moves 1 position to the left or right. Check both directions and all LEDs.

Digit keys:

- The corresponding digit appears in all positions of the display and the plus sign appears in the level display.

Decimal point:

- Two decimal points appear in the level display.

Minus key:

- The minus sign appears in the level display.

CLR pushbutton:

- The digits 1 to 4 appear in the level display.

7.6.3.7 Interface test

With the aid of the signature analyzer, it is possible to determine to a good degree of accuracy whether the interfaces between the CPU motherboard (2) and the remaining parts of the instrument are operating correctly. The measurements are carried out on board (2).

First measuring series

Set the following on the CPU mother board (2):

- Set S 1/1 to S 1/5 to the open position
- Disconnect flat cables a, u, v
- Switch on the instrument

The level display now indicates "P--1". Even if this does not appear, faultfinding may still be possible.

Connection of the signature analyzer:

- Start to TP 2 on the CPU board (90), edge ⌝
- Stop to TP 5 on the CPU board (90), edge ⌝
- Clock to TP 2 on the CPU motherboard (2), edge ⌞
- Short circuit 2 R 59 on the CPU motherboard (2) with a test cable
- Signature after reset in probe: 6929

For the measurement, it is immaterial whether the corresponding cable is inserted or not.

Pin 4	2985
5	U1P6
6	032A
8	014F
9	3FHA
10	A8FO
11	OA61

Figure 7-16
Signatures at socket a

Pin 3	F79C
4	0530
6	996A
9	5P3F
10	89AU
11	FO29
12	APO1

Figure 7-17
Signatures at socket v

Pin 1	UHH1
2	1P6H
4	78U3
6	U623
7	OOA6

Figure 7-18
Signatures at socket u

Pin 8	8053
9	5FO2
10	C805
11	A824
12	14F2

Pin 1	1A65
2	1835
3	824F
4	33HH
5	OHCH
6	U798
11	0000
16	6929

Figure 7-19
Signatures at socket c (1st series)

Pin 1	U798
2	OA99
3	OHCH
4	824F
5	1835
6	33HH
7	1A65
16	FOFU

Figure 7-20
Signatures at socket s (1st series)

Second measuring series

Set the following on the CPU motherboard (2):

- Close S 1/1, S 1/3, S 1/4; open S 1/2, S 1/5
- Disconnect flat cables a, c, s, u and v
- Switch on the instrument.

Connection of the signature analyzer:

- Connect start and stop to pin 6 of socket a, edge
- Connect clock TP 3 on CPU motherboard (2), edge
- Signature after reset on probe: P196

Pin 7	9055
8	8AH9
13	0CH8
14	6F3F
15	4033

Figure 7-21
Signatures at socket c (2nd series)

Pin 9	Test probe flashes
10	A457
11	915H
12	48AP
13	H22C

Figure 7-22
Signatures at sockets (2nd series)

If all of the above signatures are correct, then there is almost certainly no fault on the CPU motherboard (2).

7.6.4 FAULTFINDING IN THE ANALOG SECTION

7.6.4.1 RF signals (level plan) and notes on test points

Front panel settings: P = 0 dBm/75 Ω

Output frequency: f = 20 kHz

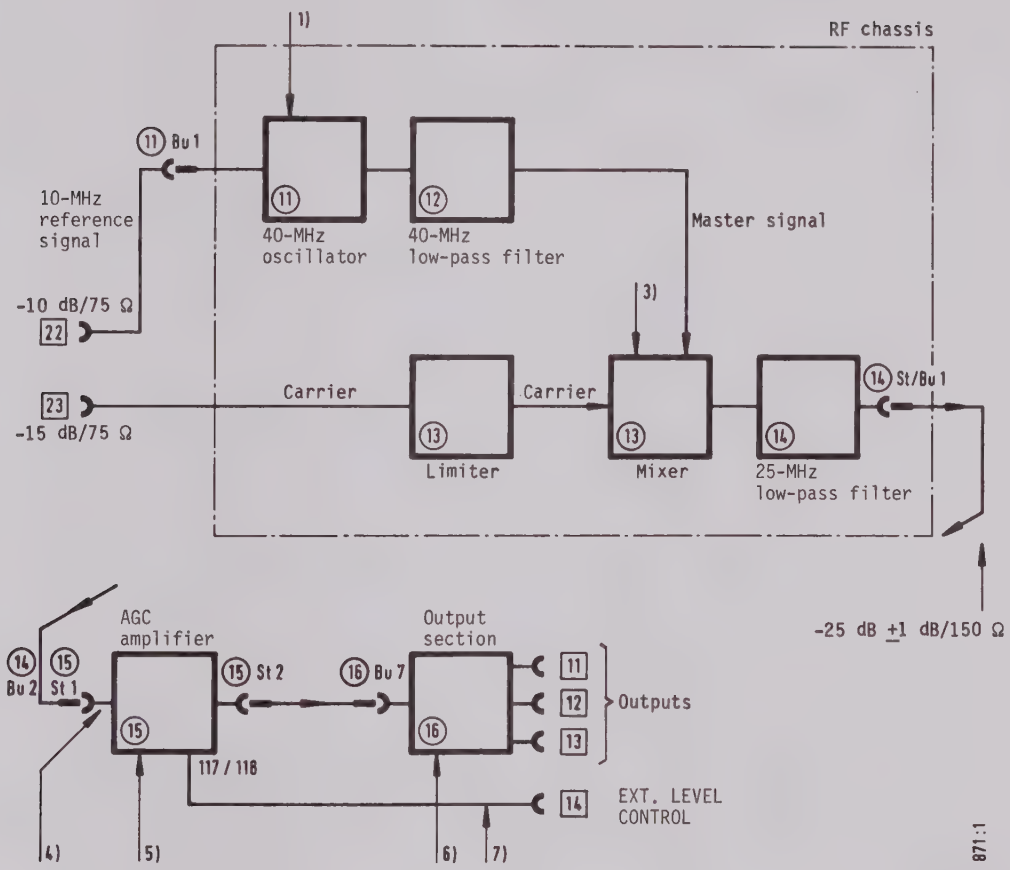


Figure 7-23 Level diagram and test points

The numbered arrows provide a cross reference to the tests in the table in Figure 7-24.

Levels are measured at high impedance with an RF mV meter.

7.6.4.2 Table of additional test points

Output frequency: 20 kHz

Test Nr.	Designation	Test conditions and settings	Measuring equipment	Test point	Nominal value/ signal shape	Possible fault or subsequent test in case of deviation
1)	Signal IN/OUT		Voltmeter or Oscilloscope	(11) 3 on [870-B] or (2) 1	+5 V: signal ON; approx 0 V (pushbutton "BLANK" depressed): signal off	Cable harness, digital section
2)	Carrier signal	Carrier connected to rear of instrument	Oscilloscope $\geq$ 150 MHz	(13) 15 and 16	$\geq$ 800 mV_{p-p}	Limiter
3)	Input level to AGC amplifier	Carrier connected to rear of instrument	Oscilloscope $\geq$ 1 MHz	BN 9091 VARI AMP (1) 5	Sinus 120 mV_{p-p} $\pm$12% ($\cong$ -25 dB $\pm$ 1 dB/ 150 Ω)	Check level when terminated with 150 Ω
4)	Activation of AGC amplifier	Carrier connected to rear of instrument	Voltmeter or oscilloscope or logic tester	BN 9091 Sockets a and b	see Tables in Fig. 7-29 to Fig. 7-32	Cables or digital section
5)	Activation of output section	Carrier connected to rear of instrument	Voltmeter or oscilloscope or logic tester	(3) Bu a	see Tables Fig. 7-33 and 7-34	Cables or digital section
6)	Operating point of AGC amplifier	Carrier connected to rear of instrument Level 0 dBm $\downarrow$ Level +0.1 dBm $\downarrow$ Pushbutton "BLANK" depressed	Voltmeter Z_{in} > 1 MΩ	Bu [22] EXT. LEVEL C.	approx. +1.1 ... +1.5 V Causes further rise by approx. +70 mV Causes further rise by approx. +40 mV	Cable from (15) 117 and 118 to Bu [22] Otherwise check AGC amplifier in accordance with Section 7.6.4.5.

Figure 7-24 Table of additional test points

7.6.4.3 Control of the AGC amplifier BN 9091/01

Socket	a	9091-7507
-0.1 dB	1	U 705, 11
-0.2 dB	2	U 705, 10
+5.8 V out	3	C 705; U 703-, U 704-, U 705-, 16
-0.4 dB	4	U 705, 9
No Connection	5	No Connection
Blanking	6	U 705, 6
-2 dB	7	U 704, 9
Corr. # 1 *)	8	U 703, 11
-20 dB *)	9	U 703, 10
-4 dB	10	U 703, 9
-0.8 dB	11	U 704, 11
-1 dB	12	U 704, 10
0.01 dB Steps	13	R 615
Ground	14	Ground

Pos. Logic, Ref. Level BCD coded

*)

a 8	a 9	
0	0	0 dB
1	0	+0.03 dB (Correction #1)
0	1	-20 dB
1	1	-0.04 dB (Correction #2)

Figure 7-25 Pin assignments of socket a

Socket	b	9091-7508
No Connection	1	No Connection
No Connection	2	No Connection
5 dB Feedback	3	U 803, 11
20 dB #1	4	U 803, 7
No Connection	5	No Connection
10 dB	6	U 803, 5
No Connection	7	No Connection
+12 Volt out	8	+12 V U 801, 3 ..., U 802, 3 ...
5 dB	9	U 803, 3
Fast / $\overline{\text{Slow}}$ **)	10	U 801, 9
20 dB #2	11	U 803, 9
20 dB #3	12	U 803, 14
Control Voltage Monitor	13	(8) 94 ⟶ ((9) 116)
Ground	14	Ground

**)

H	Fast
L	Slow

Figure 7-26 Pin assignments of socket b

TRUTH TABLE FOR R.F. ATTENUATORS								
OUTPUT LEVEL RANGE	OUTPUT ATTN.	FEEDBACK ATTN.	PINS ON BUFFER BOARD (8)					
			b 3	b 9	b 6	b 4	b 11	b 12
(dBm)	(dB)	(dB)	5 dB F.B.	5 dB	10 dB	20 dB #1	20 dB #2	20 dB #3
+10 ... +5.1	0	5	1	0	0	0	0	0
+5 ... +0.1	0	0	0	0	0	0	0	0
0 ... -4.9	5	0	0	1	0	0	0	0
-5 ... -9.9	10	0	0	0	1	0	0	0
-10 ... -14.9	15	0	0	1	1	0	0	0
-15 ... -19.9	20	0	0	0	0	1	0	0
-20 ... -24.9	25	0	0	1	0	1	0	0
-25 ... -29.9	30	0	0	0	1	1	0	0
-30 ... -34.9	35	0	0	1	1	1	0	0
-35 ... -39.9	40	0	0	0	0	1	1	0
-40 ... -44.9	45	0	0	1	0	1	1	0
-45 ... -49.9	50	0	0	0	1	1	1	0
-50 ... -54.9	55	0	0	1	1	1	1	0
-55 ... -59.9	60	0	0	0	0	1	1	1
-60 ... -64.9	65	0	0	1	0	1	1	1
-65 ... -69.9	70	0	0	0	1	1	1	1
-70 ... -74.9	75	0	0	1	1	1	1	1

Figure 7-27 Table for attenuators

	UNBAL [19]		BAL. I [20]				BAL. II [21]							
Z_{out}/Z	75 Ω		124 Ω		150 Ω		150/150 Ω		0/150 Ω		600/600 Ω		0/600 Ω	
Pin \ Socket	a	b	a	b	a	b	a	b	a	b	a	b	a	b
1	0	NC	0	NC	1	NC	0	NC	1	NC	0	NC	0	NC
2	0	NC	1	NC	1	NC	0	NC	0	NC	0	NC	0	NC
3	+)	0	+)	0	+)	0	+)	0	+)	0	+)	1	+)	0
4	0	0	1	0	1	0	0	0	0	0	0	0	0	0
5	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	NC	0	NC	1	NC	1	NC	1	NC	0	NC	1	NC
8	0	+12V	1	+12V	1	+12V	0	+12V	0	+12V	1	+12V	1	+12V
9	0	1	0	0	1	0	0	0	0	1	0	0	0	0
10	0	X	1	X	0	X	0	X	0	X	0	X	0	X
11	0	0	0	0	0	0	0	0	1	0	0	0	0	0
12	0	0	0	0	1	0	0	0	0	0	1	0	0	0
13	X	++)	X	++)	X	++)	X	++)	X	++)	X	++)	X	++)
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 7-28 Control signals for AGC amplifier BN 9091/1, sockets a and b (corresponding to u and v on CPU motherboard) for output level 0 dBm

N.C. = no Connection
X = any
+) = see Figure 7-25
++) = see Figure 7-26

7.6.4.4 Control of the output section by the computer

PIN	4	10	5	9	6	8
Output \ Rel.	5	4	3	2	1	6
75 Ω UNBAL	H	L	L	L	L	L
124 Ω BAL I	L	H	L	L	L	L
150 Ω BAL I	L	H	H	L	L	L
150 Ω BAL II	L	L	L	H	L	H
0 Ω BAL II	L	L	L	L	H	H
*600 Ω BAL II	L	L	L	L	L	L
0 Ω BAL II	L	L	L	L	H	L
Meaning	a	b	c	d	e	f

← Remaining pins: Figure 7-31

H ≙ high (+5 V)
L ≙ low (0 V)

* This output is switched through if no signal is connected to the output section

Figure 7-29 Signals at 3 Bu a

Functions of relays 1-6

a) Rel. 5 switches between BAL. and UNBAL.
b) Rel. 4 switches between BAL. II and BAL. I
c) Rel. 3 switches between BAL. I 124 Ω and 150 Ω
d) Rel. 2 switches between BAL. II Z_o = 600 Ω and 150 Ω
e) Rel. 1 switches between $Z_{out} = Z_o$ and Z_{out} = 0
f) Rel. 6 connects correction values for Z_{out} = 0/150 Ω BAL. II

Figure 7-30 Functions of the relays

Pin 1 and 14: +12 V
Pin 2 and 7: 0 V
Pin 3 and 12: -12 V
Pin 11 (with relay 8) connects the 10 dB excess level: excess level on: H
excess level off: L

Check excess level at pin 11:
Select output BAL. II 150 Ω/150 Ω with S [7]
Level 0.0 dBm : pin 11 L
+10.0 dBm: pin 11 H

Figure 7-31 Signals at 3 Bu a

7.6.4.5 Faults in the AGC amplifier BN 9091/01

This section describes a procedure which first checks the correct connection conditions and then tests the functions of the various assemblies.

1.) Connection conditions

- Supply voltages and their connections to the modules (feed-through capacitors);
- Control signals (see also Section 7.6.4.3);
- Subminax plugs, sockets and cables at signal input and output;
- Check the input signal level with its nominal termination of 150 Ω:

should be -25 dB ± 1 dB into 150 Ω

If there is a deviation, this level should first be adjusted (see Section 7.7.3).

2.) Working points

Put the AGC amplifier into service and set up a level of 0 dBm/75 Ω.

Measure all DC voltages specified in the circuit diagram.

If deviations occur in modules which belong to the control loop (e.g. "control loop fully driven"), it is best to disconnect the control loop and proceed with testing in accordance with Section 7.6.4.5; 4.

3.) Signal levels

Operate the AGC amplifier at a frequency of 20 kHz. The following table in Figure 7-32 shows the RF levels at important points within the AGC amplifier.

Measurements with high impedance level meter in dB

Test point	Selected level in dBm	Expected level in dB	Comments
(1) 5	0.0	-25	Input impedance and the measured value from instrument to instrument; permissible deviation ±1.7 dB
(1) Q1 at base	0.0 • • • -4.9	Approx. -33.5 • • • Approx. -38.4	Measured value varies as selected level is switched from 0 to -4.9 dBm
(1) 3 (output)	0.0 • • • -4.9	Approx. -22.4 • • • Approx. -27.3	Measured value varies as selected level is switched from 0 to -4.9 dBm
(2) Q4 Emitter	0.0 • • • -4.9	Approx. +2.2 • • • Approx. -2.7	Measured value varies as selected level is switched from 0 to -4.9 dBm
(2) 14 OUTPUT A	0.0 • • • -4.9	-3.6 • • • Approx. -8.5	Measured value varies as selected level is switched from 0 to -4.9 dBm
(2) 15 OUTPUT B	0.0 • • • -4.9	Approx. -3.1 • • • Approx. -8.0	Measured value varies as selected level is switched from 0 to -4.9 dBm
(4) 48 (= 5 R 15)	0.0 • • • -4.9	Approx. -8.1 • • • Approx. -13	Measured value varies as selected level is switched from 0 to -4.9 dBm
(5) R 14	0.0 • • • -4.9	Approx. -21.1 • • • Approx. -26.8	Measured value varies as selected level is switched from 0 to -4.9 dBm
(5) 57 (= (5) R 7) (= (7) 73)	0.0 • • • -4.9	Approx. -8 • • • Approx. -12.9	Measured value varies as selected level is switched from 0 to -4.9 dBm
(5) R 8	0.0 • • • -4.9	Approx. -21.1 • • • Approx. -26.8	Measured value varies as selected level is switched from 0 to -4.9 dBm
(7) U1,1	0.0	Approx. -2.8	
(7) U1,7	0.0	Approx. -2.8	
(7) U2,7	0.0	Approx. -2.9	
(7) U2,1	0.0	Approx. -2.75	
(7) TP 3		Approx. -3.0	

Figure 7-32 Levels in the AGC amplifier

4.) Open control loop measurements

Unsolder 9 R 12 and connect a DC voltage source with $Z_{out} \leq 200\ \Omega$ to the solder terminal leading to 9 C 4 and (9) 114.

Set to the required value of + 1.73 V ± 50 mV:

Module (1) - vari-amp - is at its normal working point.

At the correct RF input level, the levels specified in Section 7.6.5; 3. must now exist.

The function of the vari-amp can be checked by varying the DC voltage as shown in the following table.

External DC voltage ("Control voltage")	Output level into 75 Ω	Remarks
Approx. ≤ +0.5 V	Approx. +5 dBm	Maximum level; "upper limit"
Approx. +1 V	Approx. +4 dBm	Operating range: approximately linear working range
+1.73 V	0 dBm	
Approx. +2 V	Approx. -6 dBm	
Approx. ≥ +2.5 V	Approx. ≤ -16 dBm	

Figure 7-33 Characteristic of the vari-amp

7.6.4.6 Repairs that the user can carry out

The following list shows how each each module can be repaired and, if applicable, which realignment is necessary afterwards.

(1) VARI-AMP

Components in the control path can be repaced, but not those in the RF signal path.

(2) POWER AMP

Transistors in RF path Q4, Q5 and Q6 can be replaced. If necessary, check the distortion adjustment.

Relays may not be replaced!

(3) WIDE-BAND ATTENUATOR

Only functional check possible; do not repair.

(4) LOSS SIMULATOR

Only a functional check is possible, including switching by the relay. The relay cannot be replaced!

(5) TRACK DETECTOR

Only functional check of signal and reference paths possible.

(6) REFERENCE GENERATOR

Repair possible; subsequently check and, if necessary, adjust the absolute level 0 dBm and the rectifier linearity as specified in Section 7.7.9.

(7) REFERENCE ATTENUATOR
(8) RELAY BUFFER
(9) LOOP CONTROL

} Repair possible

7.6.5 FURTHER FAULTFINDING

7.6.5.1 Faults in the supply voltages

Indications of incorrect supply voltages can be:

Front panel lamps do not light or are too dim; operation of relays cannot be heard when the output sockets are switched (with switch [7]).

Procedure:

Switch off the instrument, remove the case cover, swing up the control section. Disconnect the supply voltage plugs from the output section and AGC amplifier.

Check the voltages at the solder terminals of the CPU motherboard as shown in Figure 7-34.

If the values are incorrect: unsolder +12 V and -12 V lines to the RF chassis and again check the supply voltages.

If the supply voltages are correct: Switch off the instrument, connect all supply voltages to the output section, switch on the instrument and check the voltages. Repeat this procedure for the AGC amplifier and the synthesizer.

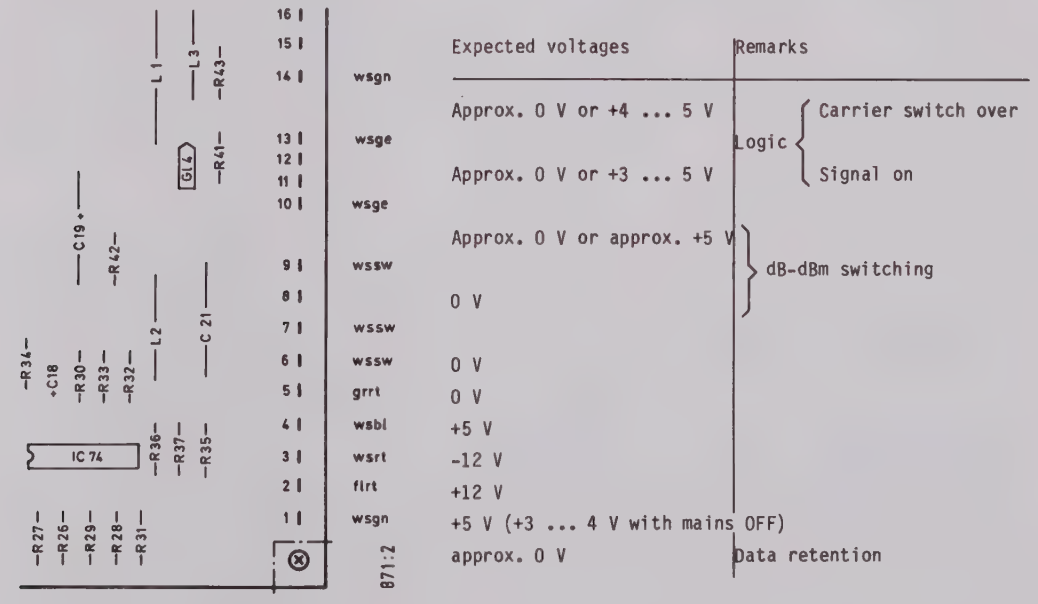


Figure 7-34 Signals at soldering tags on the CPU motherboard

If the AGC amplifier is faulty: see fault finding strategy in Section 7.6.4.3 and Section 7.6.4.4.

If the values are still incorrect: unsolder all wires carrying supply voltages to the CPU motherboard and again check the voltages.

If the CPU motherboard is faulty: check digital section in accordance with Section 7.6.2 if the standard power supply unit is faulty: see documents for BN 844

7.7 ALIGNMENT INSTRUCTIONS

7.7.1 OVERVIEW

Trimmer	Alignment	Section
11 L 1	Pulling range of 40 MHz master oscilloscope	7.7.2
11 P 1	Level of master oscillator's signal	7.7.3
16 P 1	Level 0 dBm/124 Ω at output BAL. I	7.7.4, 8.2
16 P 2	Level 0 dBm/150 Ω at output BAL. II	7.7.5, 8.2
16 P 3	10 dB excess level at output BAL. II	7.7.6, 8.3.3
16 P 4	Offset of output amplifier	7.7.7
14 L 1 to 14 L 6	Adjustment of 25 MHz low-pass filter	7.7.9
90 S 1	Switch position on CPU board	7.6.11.7
AGC amplifier module (15), (internal numbering in accordance with circuit diagrams BN 9091/01)		
5 R 5	Absolut level 0 dBm/75 Ω	7.7.8
6 R 7	Absolut level 0 dBm/75 Ω	7.7.8

Figure 7-35 List of alignment components

Module		Trimmer	Section
CPU motherboard (2)	Board [871-A]		
Input circuit (4)	Board [871-B]		
Level display (5)	Board [870-T]		
40 MHz oscillator (11)	Board [870-B]	11 L 1, 11 P 1	7.7.2, 7.7.3
Phase-locked loop (11)	Board [870-A]	11 L 1	7.7.2
Limiter (13)	Board [870-H]		
Mixer (13)	Board [870-G]	11 P 1	7.7.3
AGC amplifier (15), BN 9091/01		16 P 1, 16 P 2	7.7.4, 7.7.5
Output section (16) output 3	Board [870-O]		
Output section (16) output amplifier	Board [870-P]	16 P 2, 16 P 3 16 P 4	7.7.5, 7.7.6, 7.7.7
Output section (16) relay drivers	Board [870-Q]		
Output section (16) output 2	Board [870-R]	16 P 1	7.7.4
25 MHz low-pass filter (14)		14 L 1; 14 L 2; 14 L 3; 14 L 4; 14 L 5; 14 L 6	7.7.9
AGC amplifier (15) BN 9091/01 (see enclosed circuit diagrams)			
(5) TRACKING DETECTOR		5 R 5	7.7.8
(6) REFERENCE GENERATOR		6 R 7	7.7.8

Figure 7-36 Alignment after replacement of modules

7.7.2 PULLING RANGE OF THE 40 MHz MASTER OSCILLATOR (11 L 1)

Remove the baseplate of the instrument.

Required test equipment:

1 Level Generator 10 MHz	PS-6, 14, 19, 60	W & G
1 oscilloscope	PM 3260 or similar	Philips
1 digital frequency meter	PM 6614/05	Philips

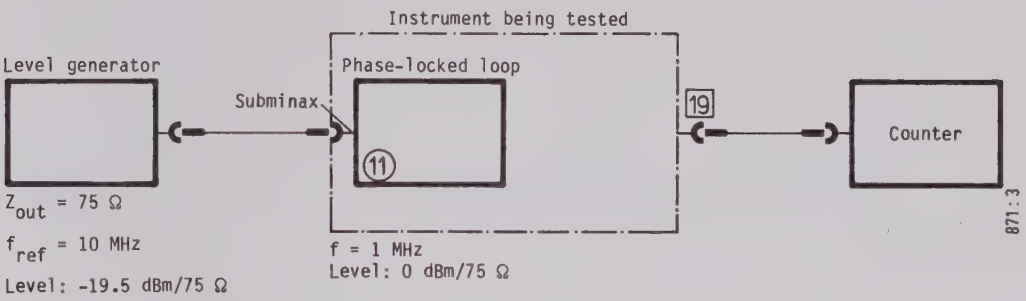


Figure 7-37 Test configuration for pulling range of master oscillator

The level generator supplies the reference frequency for the phase-locked loop. If the reference frequency is varied by ±300 kHz, the output frequency of the unit being tested must change accordingly.

The gate time of the digital frequency meter should be be set to ≤ 0.1 s.

If there is an error, realignment should be carried out with the aid of a test cover. If this is not available, the following procedure can also be used:

Slightly adjust L1 and then replace the screening cover (!) and again check the pulling range. The pulling range can be adjusted to a symmetrical value of at least ±300 kHz by repeated adjustment and measurement.

7.7.3 40 MHz MASTER OSCILLATOR LEVEL (11 P 1)

Required test equipment:

1 wide-band level meter, e.g. 400 E hp

1 terminating impedance 150 Ω

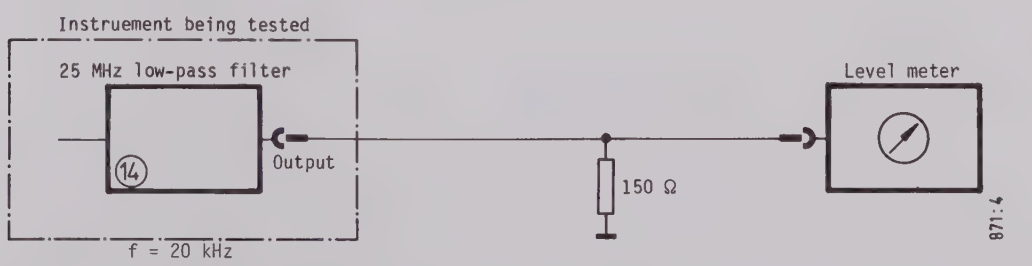


Figure 7-38 Test configuration for master oscillator level

Adjust the level to - 25 dB with 11 P 1.

7.7.4 LEVEL 0 dBm/124 Ω AT OUTPUT BAL. I (16 P 1)

Prerequisite: A value of 0.0 dBm/75 Ω ± 0.02 dB was measured (with EPM-1 and TK10) at output UNBAL [11] with f = 20 kHz and level = 0.0 dBm.
Otherwise: check/adjust as specified in Section 7.7.8.

Required test equipment:

Milliwatt Power Meter EPM-1 with TKS-10 and TKSA-124 W & G

Configuration

Figure 7-39 Test configuration for level 0 dBm/124 Ω/BAL I.

Measuring sequence:

Settings of unit being tested: select output BAL I, Z_0 = 124 Ω with S [7], frequency f = 200 kHz, level P_{out} = 0.0 dBm

Adjust the level of the output section with trimmer 16 P 1 for an indication of 0.00 dBm on the EPM-1.

7.7.5 LEVEL 0 dBm/150 Ω AT OUTPUT BAL. II (16 P 2)

Prerequisite adjustments: As for Section 7.7.4

Required test equipment:

1 mW Power Meter EPM-1 with TKS-10 and TKSA-150 Ω W & G

Test configuration:

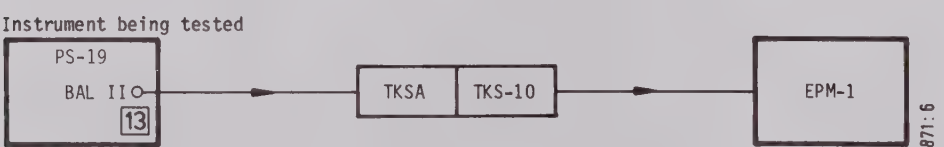


Figure 7-40 Test configuration for level 0 dBm/150 Ω/ BAL II

Measuring sequence:

Settings on instruments being tested: select output BAL II, Z_0 = 150 Ω with S [7], frequency f = 20 kHz, level 0.0 dBm

Adjust 16 P 2 of the output section for an indication of 0.00 dBm on the EPM-1.

7.7.6 EXCESS LEVEL 10 dB AT OUTPUT BAL II (16 P 3)

Prerequisite: level 0 dBm/150 Ω is calibrated (Section 7.7.5)

Required test equipment:

1 Level Meter SPM-60 W & G

Configuration

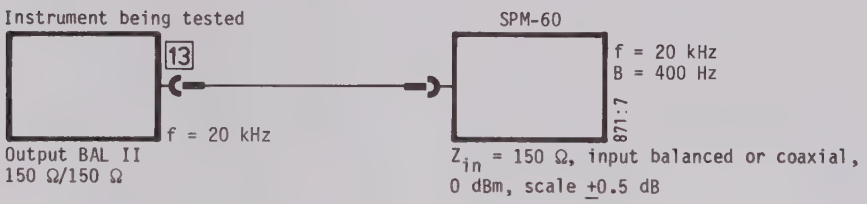


Figure 7-41 Test configuration for excess level at BAL. II

Set the output level from the instrument being tested to 0.0 dBm and adjust the scale pointer on the SPM-60 to the 0 mark.

Set the measuring range of the SPM-60 to + 10 dBm and set the output level of the instrument being tested to + 10 dBm. Adjust 16 P 3 until the indication on the SPM-60 coincides with the 0 mark.

7.7.7 OFFSET OF OUTPUT AMPLIFIER (16 P 4)

Required test equipment:

1 digital voltmeter, resolution 0.1 mV e.g. 8600 A Fluke
1 terminating impedance 75 Ω (preferably subminax)

Configuration

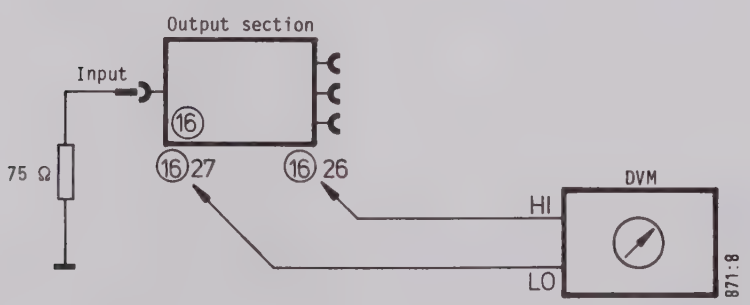


Figure 7-42 Test configuration for offset of output amplifier

Settings: level 0 dBm, output BAL II, Z_o and Z_{out} any value.
Unsolder cables from (16) 27 and (16) 26, connect the DVM, and adjust 16 P 4 for a DC voltage of 0.0 mV.

7.7.8 ABSOLUTE LEVEL 0 dBm/75 Ω

Carry out measurements and adjustments at a temperature of 23° C ± 3 K.

With the aid of the following two-point adjustment, the absolute 0 level dBm and the linearity of the rectifier characteristic in the tracking detector are adjusted.

Required test equipment:

1 Miliwattt Power Meter	EPM-1	BN 564/0	W & G
1 Test Probe	TK-10	BN 572/0	W & G
1 Level Meter	SPM-19	BN 829	W & G

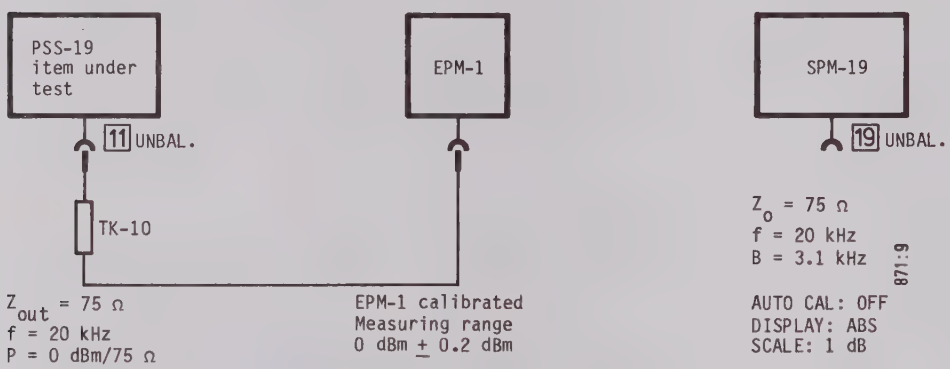


Figure 7-43 Test configuration for absolute level 0 dBm/75 Ω

7.7.8.1 Calibration of the SPM-19

Connect the EPM-1 with test probe TK-10 to Bu [11] of the instrument being tested and adjust 6 R 7 in the AGC amplifier for an indication of 0 on the EPM-1. If the adjustment range of the potentiometer is insufficient, the value of 5 R 5 can also be changed. Now connect output [11] of the instrument being tested to input [19] of the SPM-19.

A Set the SPM-19 to the measuring range 0 dBm with the following commands:
"MEM", "9213", "RCL", "9320", "RCL", "9400", "RCL"

Note the value indicated by the SPM-19. This is the 0 dBm reference point for the following two-point adjustment.

7.7.8.2 Two-point adjustment

B Set the instrument being tested to an output level of - 4.9 dBm.
Set the SPM-19 to a measuring range of - 4.9 dBm with the following commands:
"MEM", "9324", "RCL", "9409", "RCL"
Adjust 5 R 5 of the AGC amplifier for the same indication as at the 0 dBm reference point.

Set up the instrument as in A - at output level 0 dBm - and adjust 6 R 7 for the same indication as at the reference point.

Repeat steps A and B alternately until both indicated values are equal.

Finally, again connect the instrument being tested and the EPM-1 as shown in the test configuration in Figure 7-43. Any remaining deviation from 0 dBm is then removed with 6 R 7.

7.7.9 ADJUSTMENT OF THE 25 MHz LOW-PASS FILTER (14)

Alignment and testing of the low-pass filter without special test equipment is only possible under certain reservations. For this reason, alignment and checking should be carried out in the factory.

It should also be mentioned that faults in this module are extremely rare and that any changes to the factory settings of this module make checking and readjustment of the frequency response necessary.

The low-pass filter can be checked and aligned as follows, if the user is prepared to accept the extra time involved, and is ready to work with improvised test equipment.

- Remove mixer (13), [870-G]
- Disconnect the subminax connector from the AGC amplifier input (15) Pkt. 5.
- Connect an adaptor with matching pad as shown in Figure 7-45.

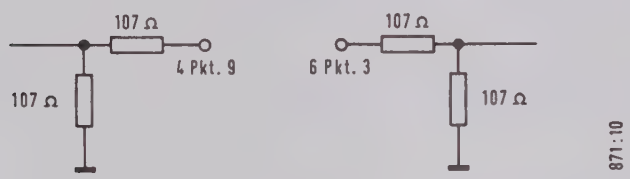


Figure 7-44 75 Ω/150 Ω matching pad

Required test equipment:

1 Level Meter	SPM-14	BN 830/0	W & G
1 Level Generator	PSS-14	BN 833/0	W & G
2 matching pads	150 Ω/75 Ω		

- If necessary, fit a cover with alignment holes instead of the normal cover of the low-pass filter

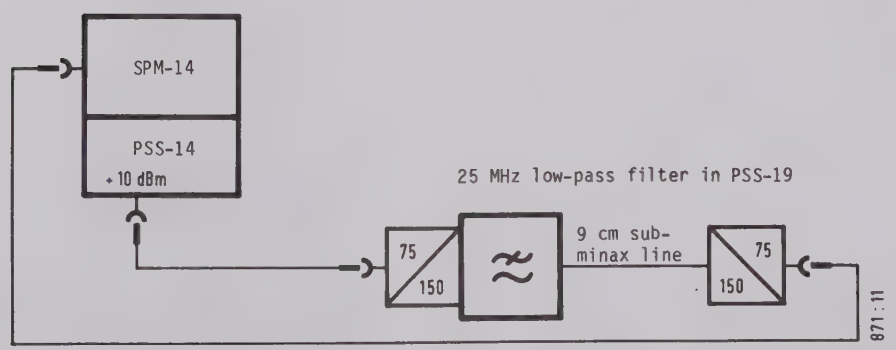
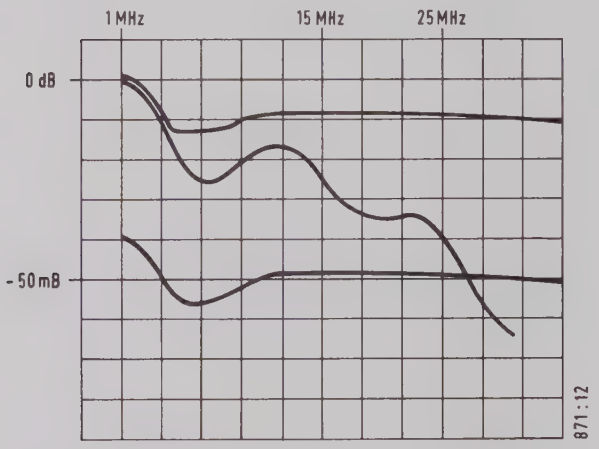


Figure 7-45 Test configuration for 25 MHz low-pass filter

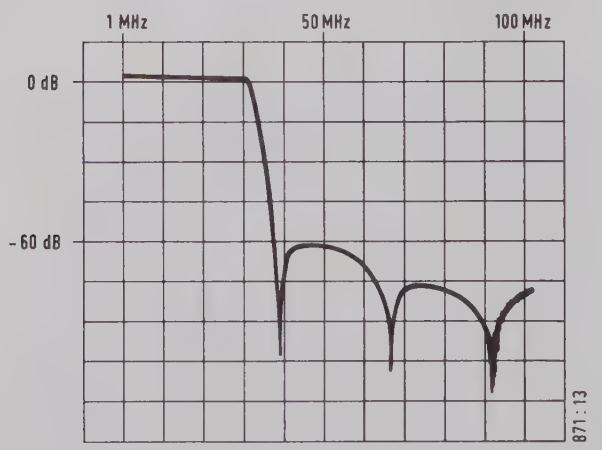
Adjustment:

- Connect the 9 cm long subminax cable to 14 Bu 1.
- First, in the measuring configuration, connect the generator output via the two adaptors (direct) to the receiver input. Output level +6 dBm. On the receiver, a reference point at approximately 1.0 MHz of -10 dBm, low noise, is then set. After this, connect the filter and cables between the two adaptors and measure the attenuation at approximately 1 MHz. This should be 0.5 ... 0.55 dB. After this, the poles are adjusted.
- Adjust the poles of the low-pass filter for maximum attenuation
  with L 1 at f = 93.280 MHz
  with L 3 at f = 60.488 MHz
  with L 4 at f = 43.759 MHz
  with L 2 at f = 40.339 MHz
- At approximately 20 MHz, L 5 and L 6 of the auxiliary low-pass filters are adjusted for minimum attenuation.
- Check the adjustment and repeat if necessary.
- Check the frequency response of the passband from 1 MHz to 25 MHz, refer to 1 MHz: this should be $\leq$ 0.4 dB



Y: 10 mB per division
X: 3 MHz per division

Figure 7-46 Aligned 25 MHz low-pass filter, passband



Y: 15 dB per division
X: 10 MHz per division

Figure 7-47 Aligned 25 MHz low-pass filter, stopband

8 CHECKING IMPORTANT SPECIFICATIONS

8.1 INTRODUCTION

This section describes procedures with which the most important characteristic values of the instruments can be checked. Wherever possible, the use of commercially-available test equipment is suggested.

Unless otherwise specified, the checks should be carried out within the nominal operating ranges of temperature and mains voltage.

If the technical data specify a warming-up period, then the tests should not be started until this time has elapsed.

Checking of the important specifications is intended to determine whether the indication of a measured parameter lies within the guaranteed error limits. This is possible without restrictions only if the intrinsic error of the test configuration used is negligible.

Otherwise, the following rules apply:

If the error of the test configuration used is $\pm m$ and if $\pm e$ is specified as the guaranteed error limit for the instrument being tested, then

a value outside the limits $\pm(e + m)$ indicates that the guaranteed error limits have definitely been exceeded;

a value within the limits $\pm(e - m)$ indicates that the error limits have definitely not been exceeded.

In each step, the values for e and m are specified. The value m depends on the test equipment used and must therefore be determined if there is any deviation from the measuring instruction.

To systematically check the data, the tests should be carried out in the sequence specified here.
Realignment of the instrument being tested should be carried out only if a value outside the limit $\pm(e + m)$ is found.

The checks in Section 8.2 and 8.3 are for detecting important partial errors of the output level.

If the output levels lie within these partial error limits, then the instrument complies with its accuracy under normal operating conditions.

Notes on instrument settings:

Unless otherwise specified, the following settings are always used:

Instrument settings:

PSS-19:

BLANK, AUTO BLANK [2], [1]:	OFF
Level unit [6]:	dBm

SPM-19:

AUTO CAL [1]:	ON
AFC [5]:	OFF
MEM [6]:	OFF
AVRG [11]:	ON

8.2 ERROR LIMITS OF THE OUTPUT LEVEL AT 0 dBm

Carry out this measurement at a temperature of 23° C ± 3 K.

Required test equipment:

1 Milliwatt Power Meter with accessories:	EPM-1	BN 564/0	W & G
1 Test Probe, 75 Ω	TK-10	BN 572/0	W & G
1 Test Probe	TKS-10	BN 668	W & G
1 Test Probe Adaptor	TKSA-124	BN 668/00.14	W & G
1 Test Probe Adaptor	TKSA-150	BN 668/00.11	W & G
1 Test Probe Adaptor	TKSA-600	BN 668/00.12	W & G
1 Calibration Adaptor	TKSE-124	BN 668/00.24	W & G
1 Calibration Adaptor	TKSE-150	BN 668/00.21	W & G
1 Calibration Adaptor	TKSE-600	BN 668/00.22	W & G

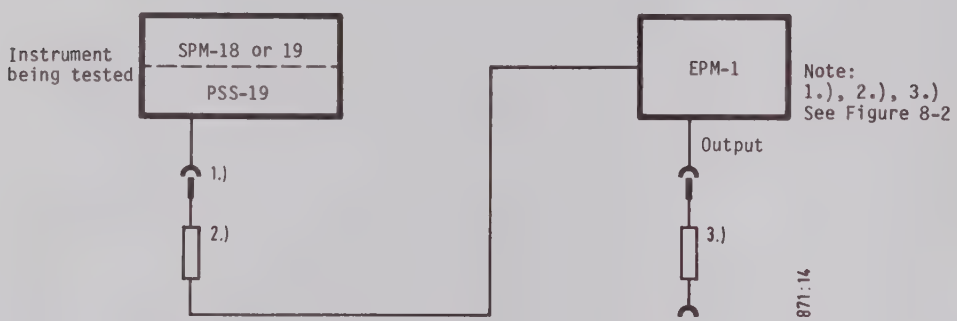


Figure 8-1 Test configuration for 0 dBm output level

Instrument settings:

PSS-19:

dB/dBm changeover switch *) [21]: dBm

Level [3], [4], [5]: 0 dBm

EPM-1:

Measuring range: 0 dBm ± 0.2 dBm

Calibration level switch when using TK-10: 0 dBm, Z_{in} = 75 Ω

Calibration level switch when using TKS-10 (Z_o = 124/150 Ω): 0 dB, Z_{in} = 0

Calibration level switch when using TKS-10 (Z_o = 600 Ω): 0 dB, Z_{in} = 75 Ω

Check all three outputs of the PSS-19 as follows, using the table (Figure 8-2):

- Calibration of the EPM-1 Milliwatt Power Meter:
  Connect the test probe to the corresponding calibration adaptor (see Figure 8-2) and adjust the meter indication to 0 with the calibration potentiometer.
- Measurement:
  Connect the test probe to the appropriate output of the PSS-19 and read off the output level from the EPM-1.

*) After changing the position of the dB/dBm switch ([21]), switch the instrument off and on again in order to make the change effective.

OUTPUT (PSS-19) [7]	Socket (PSS-19) 1.)	Frequency (SPM-18 or 19)	Test Probe (EPM-1) 2.)	Calibration Adaptor (EPM-1) 3.)	Partial error limit (e)	Error of test configuration (m)
UNBAL. 75 Ω	[11]	20 kHz	TK-10	———	±0.02 dB	±0.015 dB
BAL. I 124 Ω	[12]	200 kHz	TKS-10 with TKSA-124	TKSE-124	±0.03 dB	±0.02 dB
BAL. I 150 Ω	[12]	↓	TKS-10 with TKSA-150	TKSE-150	±0.06 dB	
BAL. II 150 Ω (Z_{out} = Z)	[13]	20 kHz	↓	↓	±0.03 dB	
BAL. II 150 Ω (Z_{out} = 0)	[13]	↓	↓	↓	±0.06 dB	
BAL. II 600 Ω (Z_{out} = Z)	[13]	↓	TKS-10 with TKSA-600	TKSE-600	±0.09 dB	
BAL. II 600 Ω (Z_{out} = 0)	[13]	↓	↓	↓	±0.06 dB	

Figure 8-2 Table for checking the 0 dBm level indication

Adjustment with 16 P 1, 16 P 2:

A prerequisite for adjustment with 16 P 1 and 16 P 2 is that the output UNBAL. 75 Ω lies within its error limits. If this output lies outside the error limits, start by adjusting the UNBAL. 75 Ω output (Section 7.7.8).

Warm-up time of instruments: > 1 hour

Output BAL. I 124 Ω: adjust with 16 P 1

Output BAL. II 150 Ω (Z_{out} = Z_o): adjust with 16 P 2

In each case, adjust for an indication for 0 dBm on the calibrated EPM-1.

8.3 ATTENUATOR ERRORS

Required test equipment:

1 Selective Level Meter	SPM-19	BN 829/xx	W & G
1 variable attenuator, Z_o = 75 Ω	D 2053	Siemens	
1 digital voltmeter	8600 A		Fluke

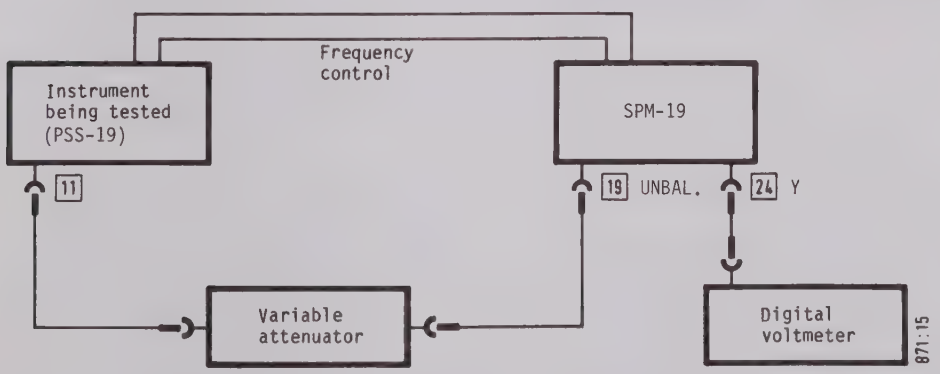


Figure 8-3 Test configuration for attenuator errors

Instrument settings:

PSS-19:

OUTPUT [7]:	Z_o = 75 Ω
Level [3], [4], [5]:	0 dBm (- 9 dB)

D 2053:

Attenuation:	40 dB (≅ 41 dB with intrinsic attenuation)

SPM-19:

dB/dBm changeover switch *) [46]:	dBm
INPUT [15]:	Z_o = 75 Ω
DISPLAY [3]:	ABS
SCALE [10]:	1 dB
Bandwidth [16]:	3.1 kHz
f [7], [12]:	20 kHz
AUTO CAL [1]:	OFF

Digital voltmeter:

Measuring range:	DCV, 20 V

8.3.1 ATTENUATION ERRORS (OUTPUT AND FEEDBACK ATTENUATORS)

These attenuators of the PSS-19 are compared with the variable attenuator of the test configuration.

Vary the output level of the PSS-19 and the setting of the variable attenuator as shown in the following Table. At each attenuator setting, determine the difference between the voltage indication (DVM) and the value noted for the reference point. The sensitivity (BB and IF gain) of the SPM-19 is not changed during the measurements. The setting at the reference points is carried out with the "MEM" pushbutton ([6], [12]) and the appropriate code number.

*) After changing the position of the dB/dBm changeover switch ([46]), switch the instrument off and on again in order to make the change effective.

Output level (PSS-19) [3], [4], [5]	Attenuator setting /dB	Divider being checked *)	Partial error limit (e) 1.)	Error of test configuration (m) 1.)
Set up following sensitivity on SPM-19: 9201 RCL, 9321 RCL, 9400 RCL				
0 dBm (-9 dB)	40	Reference point	Set reference point to 4 V ± 20 mV 2.)	———
-10 dBm (-19 dB) -20 dBm (-29 dB) -40 dBm (-49 dB) +5 dBm (-4 dB) +10 dBm (+1 dB)	30 20 0 45 50	10 dB 20 dB #1 20 dB #1, #2 5 dB 5 dB, 5 dB (F.B.)	±3.1 mB ≅ ±89 mV ±4.4 mB ≅ ±126 mV ±5.9 mB ≅ ±169 mV ±3.1 mB ≅ ±89 mV ↓	±2.5 mB ≅ ±71 mV ↓
Set up following sensitivity on SPM-19: 9202 RCL, 9331 RCL, 9400 RCL				
0 dBm (-9 dB)	60	Reference point	Set reference point to 4 V ± 20 mV 2.)	———
-60 dBm (-69 dB)	0	20 dB #1, #2 #3	±5.9 mB ≅ ±169 mV	±3.0 mB ≅ ±86 mB

*) F.B. = Feedback Attenuator
Not specified = Output Attenuator

Figure 8-4 Table for checking attenuator errors

1.) 0.01 dB ≅ 28.7 mV

2.) Setting the reference point:
The reference point must be set to 4 V ± 20 mV. For this purpose, the indication can be changed in steps of approximately 0.01 dB with the aid of the calibration control.
MEM 9398 RCL: indication increases by approximately 0.01 dB
MEM 9399 RCL: indication decreases by approximately 0.01 dB
Note the reference point for the subsequent measurements.

8.3.2 ATTENUATOR ERROR (reference attenuator)

These attenuators in the PSS-19 are compared with the IF attenuator of the SPM-19.

The external variable attenuator is not required for this measurement and is therefore removed from the test configuration (connect the SPM-19 input directly to the PSS-19 output).

Set the output levels of the PSS-19 and the sensitivity (BB and IF gain) of the SPM-19 as shown in the following table. At each attenuator setting, note the difference between the voltage indication (DVM) and the noted value of the reference point.

The wideband and IF gains of the SPM-19 required for these measurements are entered with the MEM pushbutton and the appropriate code number.

Output level (PSS-19) [3], [4], [5]	BB gain (SPM-19) /dB	MEM [6], [12]	IF gain (SPM-19) /dB	MEM [6], [12]	Stages checked	Partial error limit (e) 1.)	Error of test configuration (m) 1.)
0 dBm (-9 dB)	-30	9213 RCL	20.0	9320 RCL 9400 RCL	Ref. point	Set ref. point to 4 V ± 20 mV 2.)	———
-0.1 dBm (-9.1 dB)	↓	↓	20.1	9401 RCL	0.1 dB	±2.3 mB ≅ ±66 mV	±1.0 mB ≅ ±28 mV
-0.2 dBm (-9.2 dB)			20.2	9402 RCL	0.2 dB	↓	↓
-0.4 dBm (-9.4 dB)			20.4	9404 RCL	0.4 dB		
-0.8 dBm (-9.8 dB)			20.8	9408 RCL	0.8 dB		
0 dBm (-9 dB)	↓	↓	20.0	9320 RCL 9400 RCL	Ref. point	Set ref. point to 4 V ± 20 mV 2.)	———
-1 dBm (-10 dB)	↓	↓	21.0	9321 RCL	1 dB	±2.3 mB ≅ ±66 mV	±1.5 mB ≅ ±42 mV
-2 dBm (-11 dB)			22.0	9322 RCL	2 dB	↓	↓
-4 dBm (-19 dB)			24.0	9324 RCL	4 dB		

Figure 8-5 Table for checking attenuator errors

1.) 2.) see 8.3.1

8.3.3 ATTENUATOR ERRORS (10 dB AMPLIFIER, OUTPUT SECTION)

Required test equipment:

1 Selective Level Meter SPM-19 BN 829/xx W & G
1 digital voltmeter 8600 A Fluke

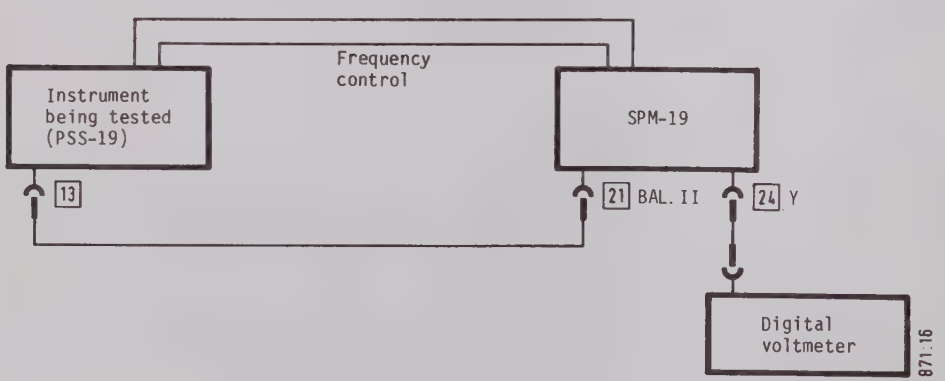


Figure 8-6 Test configuration for attenuator errors in the 10 dB amplifier

Instrument settings:

PSS-19:

OUTPUT [7]: BAL. II, Z_o = 150 Ω $Z_{out} = Z_o$

Level [3], [4], [5]: 0 dBm (-6 dB)

SPM-19:

dB/dBm changeover switch *) [46]:	dBm
INPUT [15]:	BAL. II, Z_o = 150 Ω (Z_{out} = Z_o)
DISPLAY [3]:	ABS
SCALE [10]:	1 dB
Bandwidth [16]:	3.1 kHz
f [7], [12]:	20 kHz
AUTO CAL [1]:	OFF
BB gain MEM 9213 RCL [6], [12]:	-30 dB
IF gain MEM 9325 RCL [6], [12]:	25 dB

The 10 dB amplifier of the PSS-19 is compared with the IF gain of the SPM-19:

- Set the reference point to 4 V ± 20 mV (see Section 8.3.1, 2.)
- Increase the output level of the PSS-19 to +10 dBm (+4 dB)
- Decrease the IF gain of the SPM-19 by 10 dB (MEM [6], [12]: 9315 RCL)
- Read off the deviation from the previously noted reference point on the digital voltmeter

Partial error limit (e): ±1 mB ≙ ±29 mV

Error of test configuration (m): ±2.4 mB ≙ ±70 mV

Note: Resolution of this error is not 100% accurate with the test configuration shown here. In the factory, the instrument is adjusted with specially developed test equipment.

Adjustment with 16 P 3:

Adjust 16 P 3 for an indication at the previously noted reference point. A prerequisite for adjustment of 16 P 3 is that the output BAL. II lies within the error limits of the 0 dBm output level (Section 8.2).

8.4 FREQUENCY RESPONSE OF OUTPUT LEVEL

Required test equipment:

1 Milliwatt Power Meter with accessories:	EPM-1	BN 564/0	W & G
1 Test Probe, 75 Ω	TK-10	BN 572/0	W & G
1 Test Probe	TKS-10	BN 668	W & G
1 Test Probe Adaptor	TKSA-124	BN 668/00.14	W & G
1 Test Probe Adaptor	TKSA-150	BN 668/00.11	W & G
1 Test Probe Adaptor	TKSA-600	BN 668/00.12	W & G

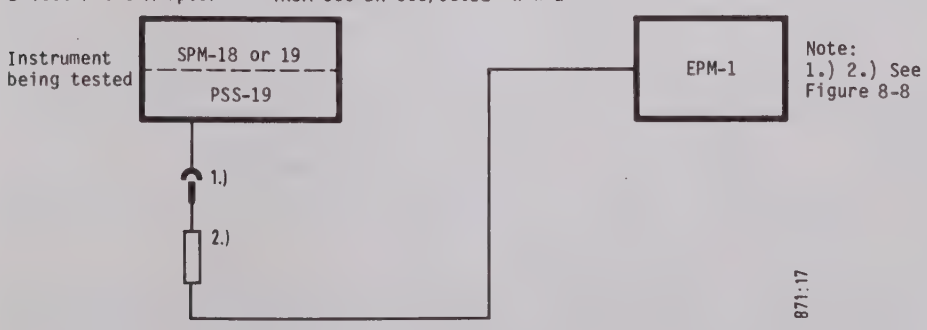


Figure 8-7 Test configuration for frequency response

*) After changing the position of the dB/dBm switch ([46]) switch the instrument off and on again in order to activate the change.

Instrument settings:

PSS-19:
dB/dBm changeover switch *) [21]: dBm
Level [3], [4], [5]: 0 dBm

EPM-1:
Measuring range: 0 dBm ±0.2 dBm

*) After changing the position of the dB/dBm switch ([21]), switch the instrument off and on in order to activate the change.

Check all three outputs of the PSS-19 as follows using the Table (Figure 8-8):

- Set up the reference frequency on the SPM-18 or 19 (see Figure 8-8).
- Adjust the calibration potentiometer of the EPM-1 for an indication of 0 (reference point)
- Read off the indication on the EPM-1 at the frequencies specified in Figure 8-8.

OUTPUT (PSS-19) [7]	Socket (PSS-19) 1.)	Test Probe (EPM-1) 2.)	Ref. frequency /kHz (SPM-18 or 19)	Meas. frequency (SPM-18 or 19)	Error limit (e) /dB	Error of test configuration (m) /dB
UNBAL. Z_o = 75 Ω	[11]	TK-10	20	80 Hz	±0.25	±0.01 dB
				200 Hz	±0.1	
				1; 100 kHz; 5 MHz	±0.08	
				25 MHz	±0.1	
BAL. I Z_o = 124 Ω	[12]	TKS-10 with TKSA-124	200	60; 500 kHz; 5 MHz	±0.15	+0.02/-0.03
				12 MHz	±0.2	
				14 MHz		*)
BAL. I Z_o = 150 Ω		TKS-10 with TKSA-150		60; 500 kHz 2 MHz	±0.15	+0.02/-0.03
				5 MHz		*)
				14 MHz	±0.2	
BAL. II Z_o = 150 Ω ($Z_{out} = Z_o$)	[13]	TKS-10 with TKSA-150	20	80 Hz	±0.25	±0.01
				200 Hz	±0.15	
				1; 100 kHz	±0.13	
				620 kHz	±0.25	
BAL. II Z_o = 600 Ω ($Z_{out} = Z_o$)		TKS-10 with TKSA-600		80 Hz	±0.25	+0.02/-0.03
				200 Hz	±0.15	
				1; 100 kHz	±0.13	
				620 kHz	±0.25	

*) Here, there may be a slight increase in the error of the test configuration, as the errors of the EPM-1 in this frequency range are no longer guaranteed by its characteristic values.

Figure 8-8 Table for checking frequency response for the output level

8.5 RETURN LOSS

Measurement notes:

The return loss at the outputs UNBAL. and BAL. I of the PSS-19 is checked in various positions of the output attenuator. This is achieved by selecting a suitable output level. In order to avoid interference coming from the AGC amplifier, it is necessary to blank the output level for the various measurements. The attenuator settings remain unaffected by this.

The measurements are carried out at the following attenuator settings: 10, 15, 20, 25 dB. At output attenuator settings of < 10 dB, the AGC amplifier causes incorrect results. Measurements at output attenuator settings > 25 dB do not need to be carried out, as the additional attenuator which is connected in these cases has no further effect on the return loss.

The return loss of output BAL. II does not depend on the output attenuator setting (buffer amplifier!), which means that only one measurement at one attenuator setting is necessary.

8.5.1 RETURN LOSS OF OUTPUT UNBAL.

Required test equipment:

1 Selective Level Meter	SPM-19	BN 829/xx (series D or later)	W & G
1 Return Loss Coefficient Measurement Bridge	RFZ-14	BN 830/00.01	W & G

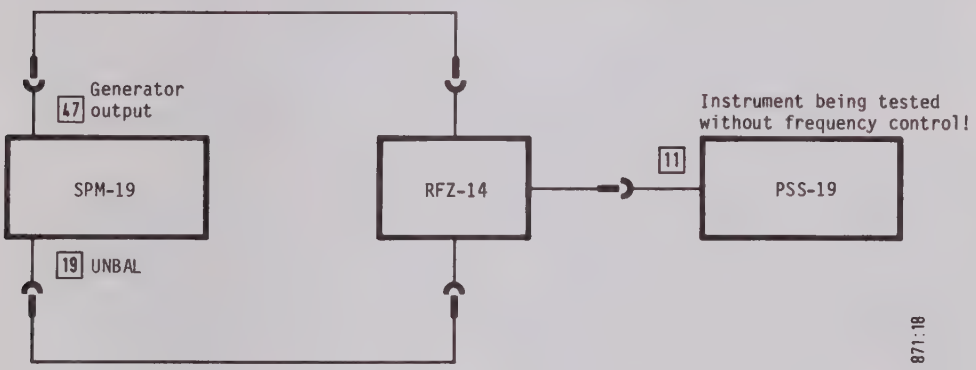


Figure 8-9 Test configuration for return loss of output UNBAL

Instrument settings:

PSS-19:

OUTPUT [7]:	Z_0 = 75 Ω
Level [3], [4], [5]:	-5 dBm (-14 dB)

SPM-19:

INPUT [15]:	Z_0 = 75 Ω
MODE [4]:	DGTL
Bandwidth [16]:	3.1 kHz
f [7], [12]:	5 MHz

Calibration of the test configuration:

Leave the input for the instrument to be tested on the measuring bridge open. Depress the push-buttons "ABS" and"REF" on the SPM-19 simultaneously. Then depress "ABS-REF". The indication is now 0 dB (corresponding to a return loss of a_r = 0 dB).

Measurement:

Connect the instrument to be tested to the bridge. Set up the following output levels on the instrument to be tested: -5 dBm (-14 dB); -10 dBm (-19 dB); -15 dBm (-24 dB); -20 dBm (-29 dB). After input of the output level, blank the output level (depress pushbutton "BLANK" [2]) and read off the return loss on the SPM-19.

Guaranteed error limit (e): $a_r \geq 34$ dB
Error of the test configuration (m): $m_u = 3.9$ dB
$m_l = 2.8$ dB

Example for use of measuring error:
The guaranteed error limit $a_r \geq 34$ dB is certainly
- exceeded at a measured value of $a_r < 31.2$ dB $(e - m_l)$
- achieved at a measured value $a_r > 37.9$ dB $(e + m_u)$

8.5.2 RETURN LOSS OF OUTPUT BAL.

Wherever values are in square brackets, the value before the brackets applies to output BAL. I and the value in the square brackets to output BAL. II.

Required test equipment:

1 Level Generator	PS-19	BN 870/xx	W & G
1 Selective Level Meter	SPM-19	BN 829/xx	W & G
1 Return Loss Measuring Attachment	RFZ-12	BN 810/01.00	W & G

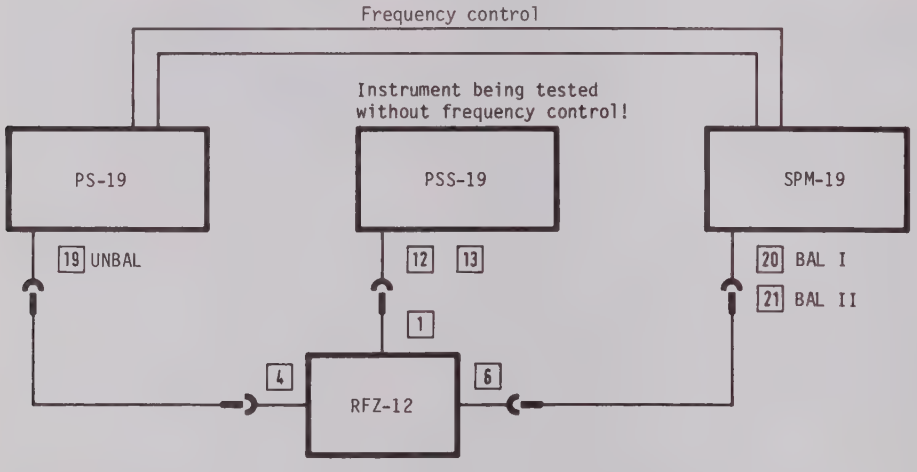


Figure 8-10 Test configuration for return loss of output BAL.

Instrument settings:

PSS-19:

OUTPUT [7]:	BAL. I (Z_0 = 124 or 150 Ω)
	[BAL. II (Z_0 = 150 or 600 Ω)]
Level [3], [4], [5]:	-7 dBm (-13 dB)

PS-19:

OUTPUT [15]:	Z_0 = 75 Ω
Level [2], [3], [4]:	+10 dBm (+1 dB)
EXT. [7]:	ON

SPM-19:

INPUT [15]:	BAL. I [BAL. II] Z_0 = 150 Ω (Z_{in} = ∞)
MODE [4]:	DGTL
Bandwidth [16]:	3.1 kHz

RFZ-12:

Operating mode [7]:	balanced

Calibration of test configuration:

Set the SPM-19 to the calibration frequency f = 60 kHz [10 kHz] with [7], [12]. Set the RFZ-12 with switch [3] to the required Z_0 value (124, 150 Ω [150, 600 Ω]) and disconnect the RFZ-12 from the instrument to be tested (input [1] open). On the SPM-19, depress pushbuttons "ABS" and "REF" simultaneously. Then depress "ABS-REF". The indication is now 0 dB (corresponding to a return loss of a_r = 0 dB).

Measurement:

Set the SPM-19 with [7], [12] to the test frequency f = 1 MHz [20 kHz] and connect the RFZ-12 to the appropriate output socket of the instrument being tested.
Set the instrument being tested to the following output levels:
Output BAL. I: -7 dBm (-13 dB); -12 dBm (-18 dB); -17 dBm (-23 dB); -22 dBm (-28 dB)
Output BAL. II: any

After inputting the output level, blank the output (depress pushbutton "BLANK" [2]), and read off the return loss on the SPM-19.

Output	Guaranteed error limit (e)	Error of test configuration (m)	
		m_u	m_l
Output BAL. I	≥ 34 dB	2.8 dB	2.3 dB
Output BAL. II			
Z_0 = 150 Ω:	≥ 34 dB	1.7 dB	1.6 dB
Z_0 = 600 Ω:	≥ 34 dB	2.8 dB	2.3 dB

Figure 8-11 Table for checking the return loss

See Section 8.5.1 for explanation of the measuring errors.

8.6 HARMONIC RATIO

8.6.1 HARMONIC RATIO, f = 200 Hz...60 kHz

Required test equipment:

1 Selective Level Meter SPM-11 BN 604 W & G
1 Terminating impedance, 75 Ω, coaxial
1 Terminating impedance, 124 Ω, balanced
1 Terminating impedance, 150 Ω, balanced

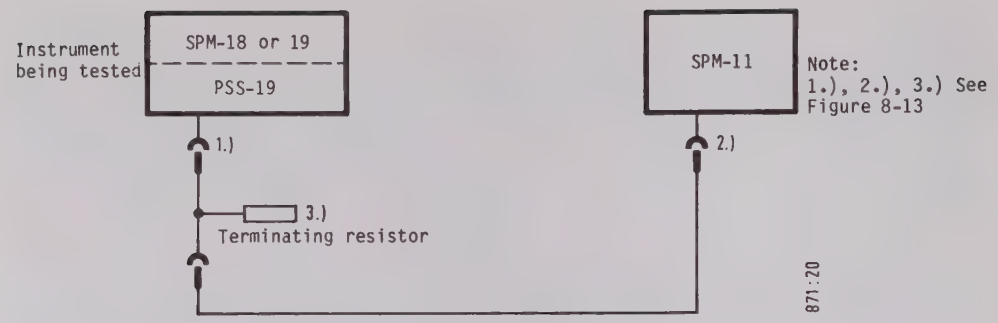


Figure 8-12 Test configuration for harmonic ratio (200 Hz to 60 kHz)

Instrument settings:

SPM-11:
Operating mode [10]: low distortion, slow
Bandwidth [6]: 8 Hz

Check all 3 outputs of the PSS-19 as follows, using the table (Figure 8-13):

- Set the PSS-19 to the appropriate level and the SPM-18/19 to the corresponding frequency (see Figure 8-13).
- Tune the SPM-11 to the basic frequency and adjust to the reference point (0 dB mark) with the calibration potentiometer [5].
- Then tune the SPM-11 to the 2nd and 3rd harmonics. The necessary increase in the sensitivity of the SPM-11 ([3]) must not exceed 60 dB.
- Read off the harmonic ratios a_{k2} and a_{k3}.

OUTPUT (PSS-19) [7]	Socket (PSS-19) 1.)	Frequency (SPM-18/19)	Level (PSS-19) [3], [4], [5]	Terminating impedance 3.)	Socket (SPM-11) 2.)	Meas. range for basic frequency (SPM-11) [3]	Error limit (e), a_{k2}, a_{k3}/dB	Error of test configuration (m)/dB
UNBAL. Z_o = 75 Ω	[11]	200 Hz	+10 dBm (+1 dB)	75 Ω	[8]	0 dB	≥ 48	0.4
		800 Hz					≥ 50	0.4
BAL. I Z_o = 124 Ω	[12]	60 kHz	+9.6 dBm (+2.7 dB)	124 Ω	[9]	0 dB	≥ 50	0.6
BAL. II Z_o = 150 Ω (Z_{out} = 0)	[13]	200 Hz	+22.9 dBm (+16.9 dB)	150 Ω	[9]	+20 dB	≥ 46	0.4
		800 Hz					≥ 50	0.4

Figure 8-13 Table for checking the harmonic ratio

8.6.2 HARMONIC RATIO, f = 100 kHz...620 kHz

Required test equipment:

1 Selective Level Meter SPM-19 BN 829/xx W & G

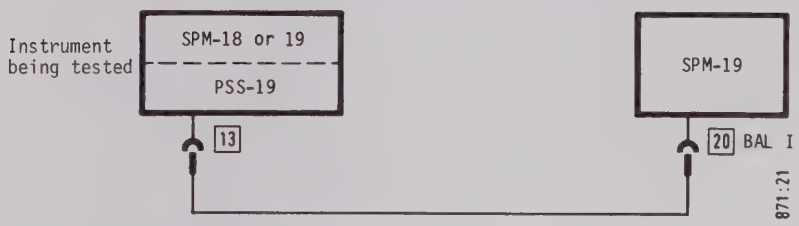


Figure 8-14 Test configuration for harmonic ratio (100 kHz to 620 kHz)

Instrument settings:

PSS-19:

OUTPUT [7]: BAL. II Z_o = 150 Ω (Z_{out} = 0)
Level [3], [4], [5]: +10 dBm (+4 dB)
Frequency (SPM-18 or 19): 100 kHz or 620 kHz

SPM-19:

INPUT [15]: BAL. I, Z_o = 150 Ω (Z_{out} = Z_o)
MODE [4]: DGTL
Bandwidth [16]: 3.1 kHz
f [7], [12]: 100 kHz or 620 kHz

On the SPM-19, depress the pushbuttons "ABS" and "REF" simultaneously. Then depress "ABS-REF". The indication is now 0.00 dB.

Tune the SPM-19 to the 2nd and 3rd harmonics of the PSS-19 output frequency and read off the harmonic ratios at a_{k2} and a_{k3}.

Increase the level of the PSS-19 to +22.9 dBm (+ 16.9 dB) and repeat the measurement.

	f = 100 kHz	f = 620 kHz
Guaranteed error limit (e): a_{k2}, a_{k3}	≥ 50 dB	≥ 46 dB
Error of test configuration (m):		
at output level + 10 dBm (+4 dB):	0.6 dB	0.5 dB
at output level + 22.9 dBm (+ 16.9 dB):	An error for the test configuration cannot be specified for this level range, as the SPM-19 is being used outside its guaranteed range.	

8.6.3 HARMONIC RATIO, f = 25 MHz

Required test equipment:

1 Selective Level Meter	SPM-14	BN 830/0	W & G
1 Attenuator, 40 dB	DG-940	BN 920/43	W & G

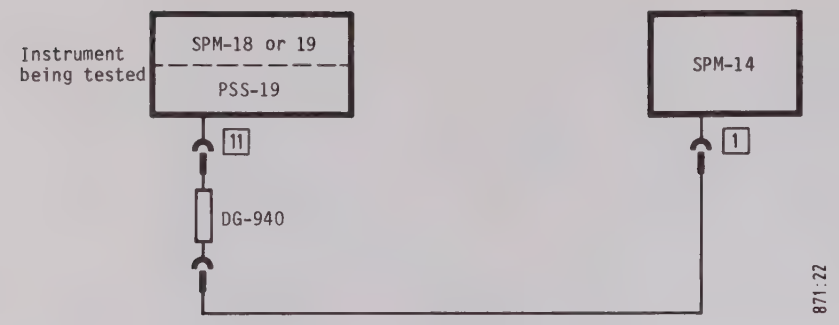


Figure 8-15 Test configuration for harmonic ratio (25 MHz)

Instrument settings:

OUTPUT [7]	Z_{out} = 75 Ω
Level [3], [4], [5]:	+ 10 dBm (+ 1 dB)
Frequency (SPM-18 or 19):	25 MHz

SPM-14:

Operating mode [7]:	low distortion
Bandwidth [8]:	2.3 kHz
Scale [6]:	- 90...0
Measuring range [5]:	0 dBm
f [33], [43]:	25 MHz

Tune the SPM-14 to the basic frequency (25 MHz). Adjust to the reference point (scale indication -30 dB) with the CAL potentiometer [4]. Then tune the SPM-14 to the 2nd (50 MHz) and 3rd 75 MHz) harmonics and read off the indication.

Guaranteed error limit (e):	a_{k2}, $a_{k3} \geq$ 50 dB
corresponds to SPM-14 indication	$\leq$ - 80 dBm
Error of test configuration (m):	3 dB

8.7 B L A N K I N G A T T E N U A T I O N

Required test equipment:

1 Selective Level Meter SPM-19 BN 829/xx W & G

Test configuration:

Connect output [11] of the PSS-19 to input [19] (UNBAL.) of the SPM-19. The PSS-19 frequency is controlled by the SPM-19.

Instrument settings:

PSS-19:

OUTPUT [7]:	Z_{out} = 75 Ω
Level [3], [4], [5]:	+10 dB (+1 dB)

SPM-19:

INPUT [15]:	Z_{in} = 75 Ω
MODE [4]:	DGTL
Bandwidth [16]:	3.1 kHz
f [7], [12]:	25 MHz

On the SPM-19, depress the pushbuttons "ABS" and "REF" simultaneously. Then depress "ABS-REF". The indication is now 0.00 dB.

Switch off the output level of the PSS-19 with "BLANK" ([2]) and read off the attenuation on the SPM-19.

Guaranteed error limit (e):	$\geq$ 80 dB
Error of the test configuration (m):	$\pm$0.2 dB

9 DESCRIPTION OF FUNCTIONS AND CIRCUITS

9.1 FUNCTIONAL DESCRIPTION OF THE COMPLETE INSTRUMENT

See block diagram 871-7500.015/33

The PSS-19 Level Generator is based on the well-known principle of the heterodyne generator and is characterized particularly by its wide frequency range of 80 Hz to 25 MHz at the coaxial output and 80 Hz to 14 MHz at the balanced output, its frequency and level accuracy, and its ease of use.

The instrument does not generate its own carrier; it receives the carrier signal and the reference frequency to generate the required output signal from the SPM-19 Selective Level Meter.

The PSS-19 has a built-in microprocessor to control all instrument functions. Withthe aid of a special data interface, the PSS-19 can be connected to the SPM-19 to form a level measuring set-up which can be used in development, installation and monitoring of multichannel carrier frequency systems down to the channel level. Even at this level, a high degree of automation of the measuring procedures is possible.

The PSS-19 Level Generator can be combined with the SPM-19 Level Meter and the standard data interface <IEC 625> of the level meter to form part of automatic production lines or computer-assisted measuring setups.

The most important instrument functions are described below using the block diagram.

The extremely simplified block diagram shows the main functional groups:

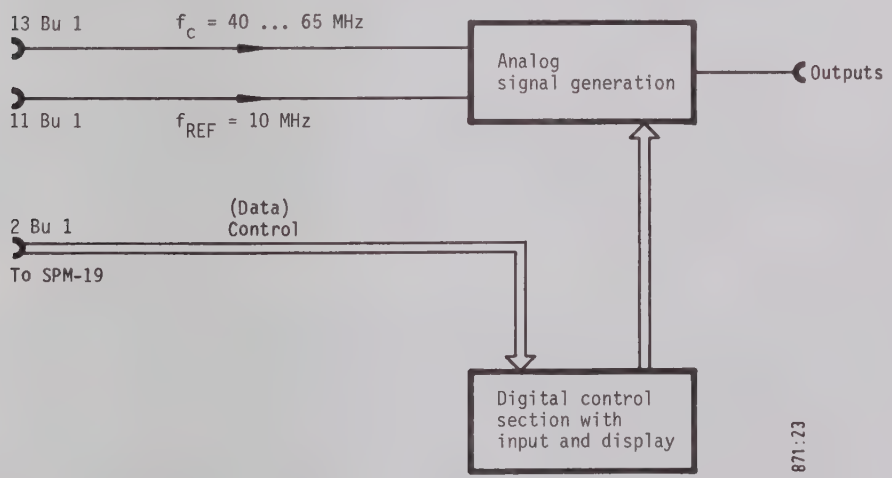


Figure 9-1 Simplified block diagram

The carrier and reference frequency and the control signals are fed by cables to the rear of the PSS-19.

9.1.1 ANALOG SECTION

The analog section of the PSS-19 consists of modules (11) to (16) and has no special features with regard to its principle of operation. Module (11) generates, in a phase-locked loop, the master frequency f_z = 40 MHz by locking to the reference frequency f_{ref} = 10 MHz. The 40 MHz value of the master frequency is determined by the design of the SPM-19 Level Meter, in which the first intermediate frequency is 40 MHz. The use of the same frequency as the master in the heterodyne generator and as the first intermediate frequency of the heterodyne receiver ensures that the generator and receiver are always tuned to precisely the same frequency when both instruments are operated with a single tuned oscillator (e.g. for sweep operation).

The 40 MHz signal generated in (11) passes through the 40 MHz low-pass filter, assembly (12), which removes almost all of the harmonics. This is necessary in order to prevent generation of specific, non-harmonic spectral lines in the following mixer.

Mixing of the 40 MHz master signal with the carrier frequency 40 MHz ... 65 MHz is carried out in assembly (13), the limiter and mixer, to which the carrier frequency voltage is connected. The output signal of the mixer is the difference between the carrier and master frequencies and is the actual output signal, which therefore lies between 0 and 25 MHz.

As the mixer, in addition to the difference between the two input signals, also generates the sum signal, residual carrier and master frequencies, and multiples thereof, all of which are undesired, the mixer is followed by the 25 MHz low-pass filter, assembly (14). This blocks all unwanted frequencies and allows only the desired signal to pass.

The signal generated in this manner corresponds in its frequency to the required output signal, but its amplitude is not yet correct. On the one hand, it is too small; on the other hand, it varies due to the frequency-dependent characteristics of the mixer and 25 MHz low-pass filter.

The signal is amplified to the required level and simultaneously regulated to a constant level by an amplitude regulation circuit in the following AGC amplifier, assembly (15). In addition to these characteristics, the amplifier also has the task of setting the required generator output level. This is achieved by a variable attenuator in the output path, which varies the level in 5 dB steps, and by means of a switchable attenuator in the reference path of the amplitude control loop. The setting range of this is 0 to - 4.9 dB in steps of 0.1 dB. In addition, 2 fine level corrections are carried out in this reference path when various output impedances are connected in dBm mode of the PSS-19.

The AGC amplifier has two further tasks. If the output signal of the PSS-19 is blanked or unblanked, then this must be carried out gradually. This "soft keying" is executed by the AGC amplifier when requested to do so by a signal on a control line. In addition, the 40 MHz oscillator (11) is switched off; this achieves the required high blanking attenuation values. The second additional task concerns the facility for external level control. For this purpose, for example via an EPM-1, it is possible to construct an amplitude control loop with socket 15 Bu 1 as the control input, via which the amplifier is controlled such that it acts as the controlling element of the external control loop.

The control loop section, module (16), which is the last element of the analog signal path, distributes the signal coming from the AGC amplifier to the various outputs. Output 1 is the direct output of the AGC amplifier (15); balancing transformers are connected to outputs 2 and 3. A further important feature exists for output 3, namely that the balancing transformer is preceded by an amplifier. This permits selection of the impedance $Z_{out} \approx 0\ \Omega$ at output 3, and also permits a level increase of 10 dB at this output.

9.1.2 DIGITAL SECTION

The digital section is described on the basis of the following block diagram.

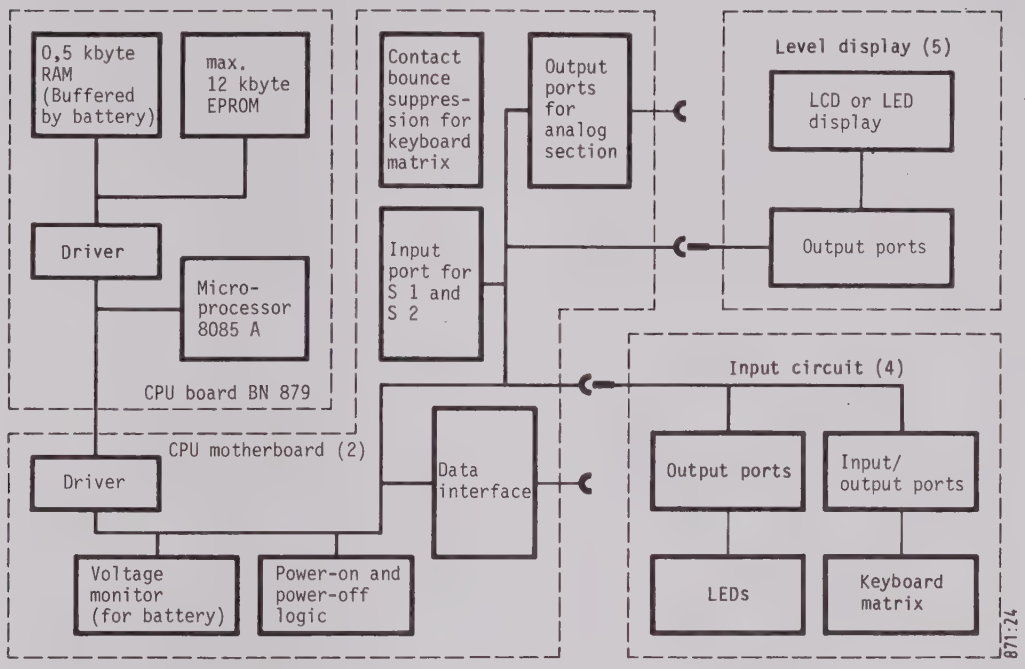


Figure 9-2 Detailed block diagram of the digital section

9.1.2.1 CPU board

The CPU board contains, in addition to the processor, the program memory and the RAM. The RAM (CMOS module) is a non-volatile memory, as it is supplied by a battery in the power supply unit when the instrument is switched off, which means that data is not lost.

9.1.2.2 CPU motherboard

The output ports are parallel interfaces to the output section and/or AGC amplifier and oscillator. With the aid of the input port, the processor can interrogate the position of switch 2 S 2 on the rear of the instrument and of the coding switches on the CPU motherboard.

The start and shutdown logic supplies the processor with a reset signal when power is switched on. In addition, the RAM is protected against uncontrolled write operations from the point where power is switched off until the power is switched on again.

The voltage monitor for the battery determines whether the RAM supply voltage with the instrument switched off is sufficient to maintain the data.

The data interface to the SPM-19 is the point where the processor bus of the SPM-19 is connected (handshake operations).

9.1.2.3 Front panel circuits

The front panel circuits consist of input and output ports for activating indicators and receiving input signals from keys and pushbuttons. The contact bounce suppression circuit for the key board matrix is located on the CPU motherboard (2).

9.2 CIRCUIT DESCRIPTION OF MODULES

9.2.1 CPU MOTHERBOARD [871-A]

9.2.1.1 Block diagram

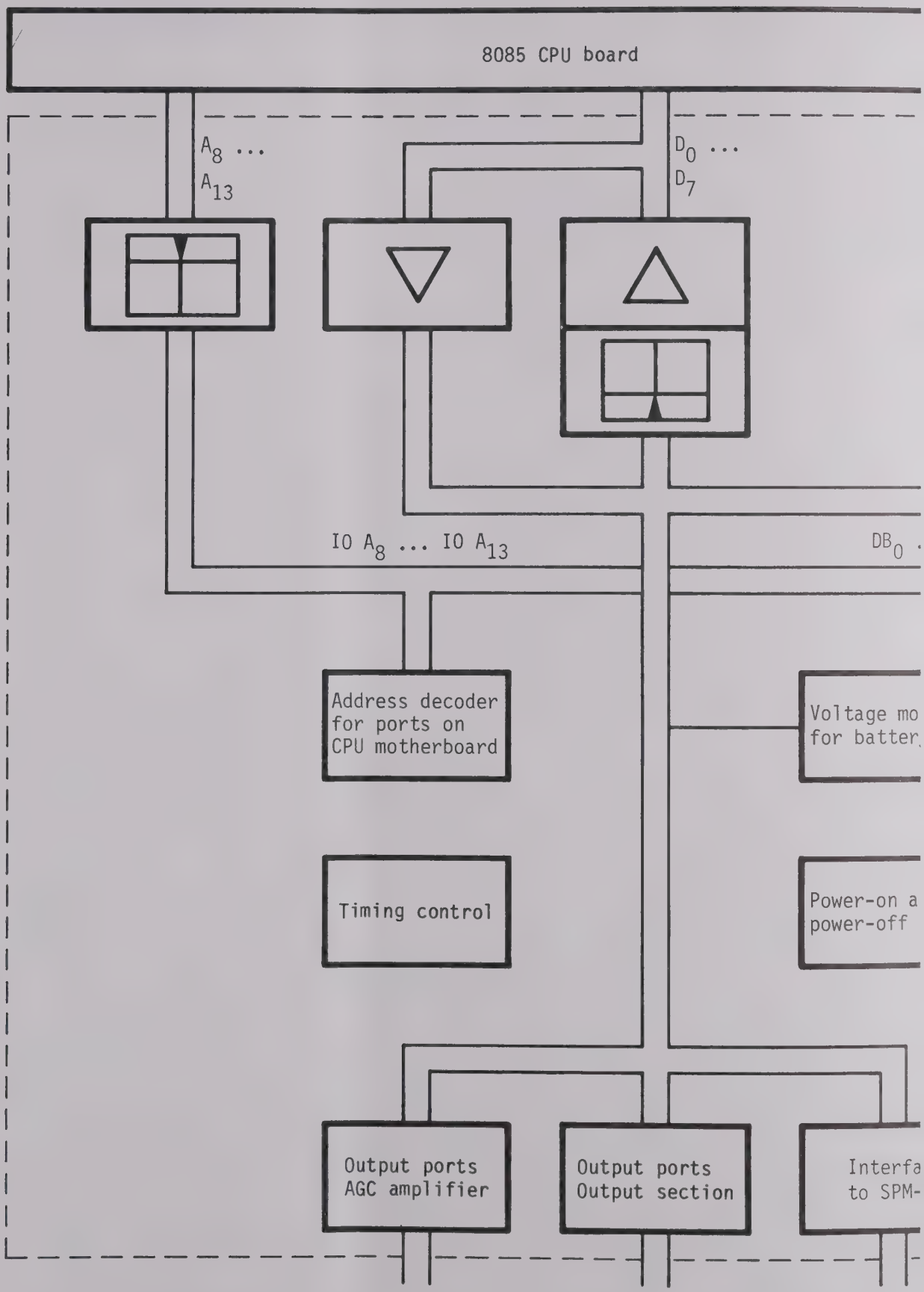
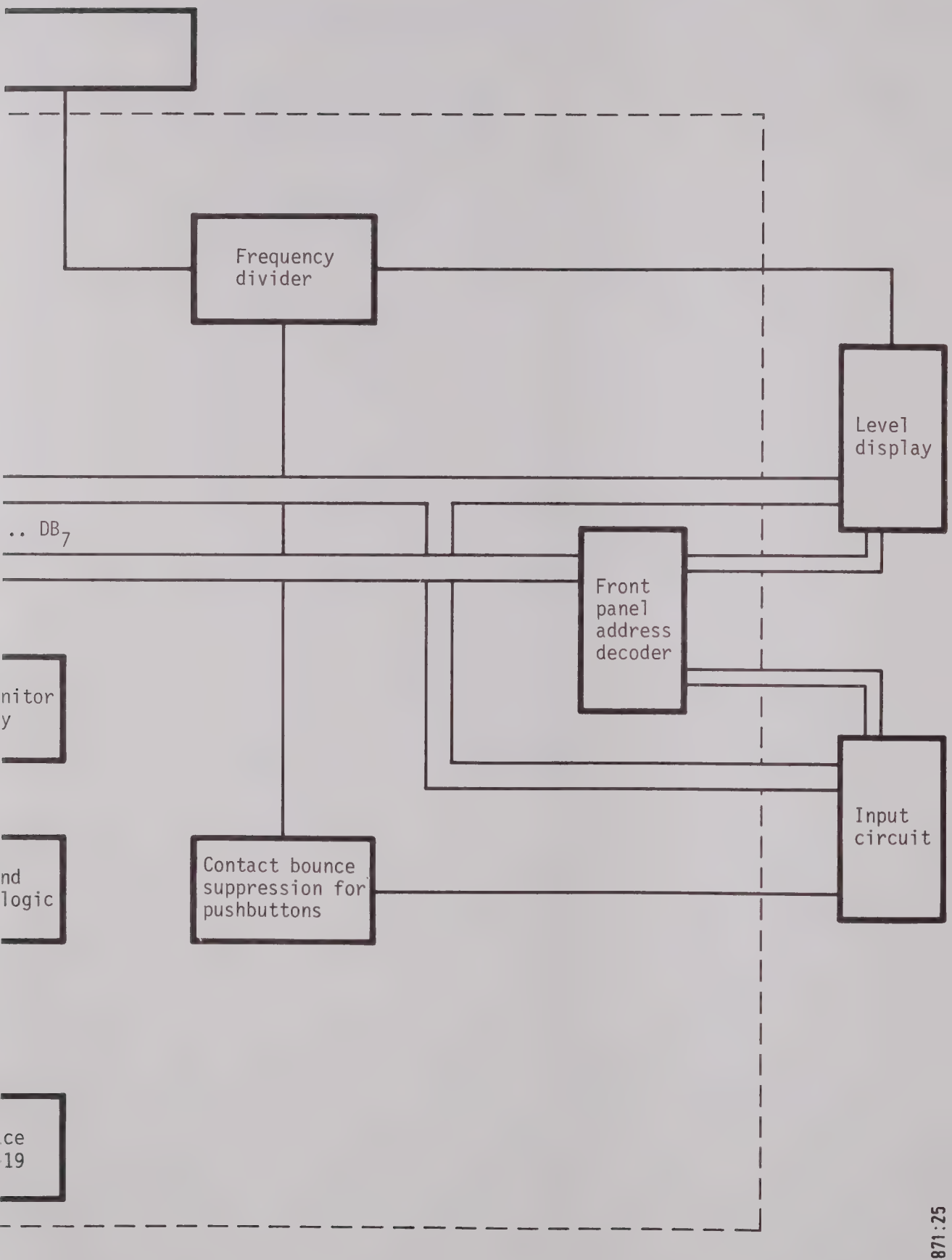


Figure 9-3 CPU motherboard


Frequency divider
Level display
.. DB7
Front panel address decoder
nitor
y
Input circuit
nd
logic
Contact bounce suppression for pushbuttons
ce
19
871:25

9.2.1.2 Drivers and latches on the 8085 interface

The address is stored in IC 1 before the actual operation is started. The remaining address bits A_{14} and A_{15} are processed in the form of the predecoder signals $\overline{V_1}$ and $\overline{V_3}$, but these are not buffered.

For each output operation, the drivers IC 10 and IC 6/2 are activated.

For each I/O operation (including output!), the data on the I/O data bus DB are stored in the latches IC 5 and IC 7. For input operations, the data are connected via IC 6/1 and IC 8/1 to the data bus of the processor AD. Output data in IC 5 and IC 7 are not evaluated.

The drivers are controlled with signals $\overline{RD_C}$ and $\overline{WR_C}$, which are active only during I/O operations.

9.2.1.3 Timing control (IC 11 to IC 15)

The following diagram is valid for input/output operations:

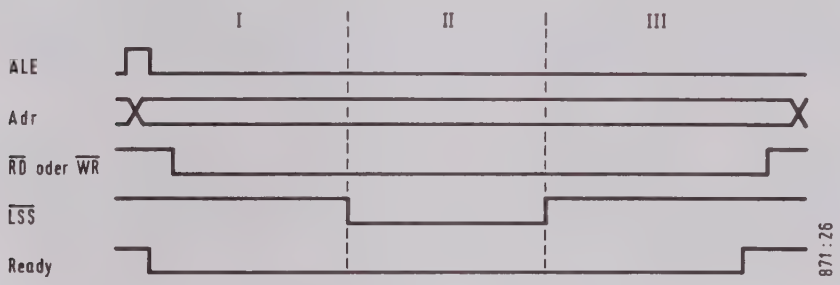


Figure 9-4 Basic timing of I/O operations.

This considerably slower sequence is necessary in order to allow the CMOS buses sufficient time to settle at the appropriate logic state.

The task of the timing control is to delay the computer with a ready signal for a sufficient period of time, to divide this time into 3 approximately equal sections, and to generate a low speed strobe (LSS).

Details of the timing control:

The ALE signal resets FFs IC 14/1, IC 15/2 and IC 14/2. As soon as a port address (IO/$\overline{M}$ = high) is present, the READY signal is set to low via IC 4/3 and IC 4/4. The value with which counter IC 12 is loaded determines the length of each section. The clock enabled by READY via IC 11/2 and IC 11/3 sets IC 14/2, and permits the counter to start. As soon as a counter overflow occurs, IC 14/2 is set with the next positive edge, IC 14/12 is reset with the next positive edge after this, and the counter is again loaded.

When IC 14/1 returns to its original state, IC 15/1 is set and $\overline{LSS}$ switches to low. At the next counter overflow, IC 15/1 returns to its original state and IC 15/2 is set. When IC 14/1 is set during the third and last counter overflow, the READY signal is set via IC 4/4 and IC 4/3, and the I/O operation is thus complete.

When reading the port on the input circuit, the counter is loaded with a smaller value than usual during the second load operation, due to the presence of the signal $\overline{SLOW}$. This extends Section II for this operation by a further 8 clock cycles = 2.7 µs.

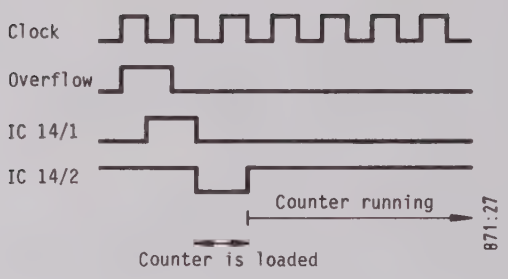


Figure 9-5 Overflow of counter IC 12

Purpose of this circuit:

Section I of the sequence is intended to allow the addresses to settle and to allow the predecoders to complete decoding, so that only the port which is actually to be addressed is activated in Section II. In Section II, the data on the data bus should settle and should be stable by the time the trailing edge of LSS appears. In Section III, the addressing logic has time to switch off the addressed port. The address lines may change their state only when this has been done.

Just as on the processor bus, where the data are valid with the training edge of the $\overline{RD}$ or $\overline{WR}$ signal on the data bus, the data in the I/O sector are valid with the trailing edge of the $\overline{LSS}$ signal. The signals $\overline{WR}$ and $\overline{RD}$ are used to a certain degree as $\overline{RD_C}$ and $\overline{WR_C}$ as status signals, i.e. for switching between writing and reading.

9.2.1.4 Frequency divider IC 17, IC 41

IC 17 is a high-speed predivider for IC 41, which generates the clock signals required for the front panel.

9.2.1.5 Address decoder for ports of the CPU motherboard IC 18, 20, 21, 24

The predecoder signal $\overline{V_3}$ (combined in IC 13/4 with I/O T_1) and the address lines IOA10 to IOA13 are decoded with IC 18/1 and IC 20/1.
Decoding of IOA_8 and IOA_9 is carried out in IC 24/1. IC 24/1 is activated via IC 21/4, during read and write operations, while $\overline{LSS}$ = low; IC 24/2 is active during write operations and IC 20/2 during read operations.

No ports in the normal sense are connected to the outputs of IC 24/1. The decoded selection signals are used as software-controlled pulses. The same applies to signal WCØ. IC 21/2 and IC 21/3 are not decoders; they are used to shorten the signals $\overline{RD_C}$ and $\overline{WR_C}$, respectively, such that they match the timing of the I/O sector.

9.2.1.6 Data interface to SPM-19 (IC 22, etc.)

The data interface is a bus interface to the processor system of the receiver SPM-19. The major part of the necessary logic is in integrated circuit 8255 (IC 22), which is programmed by the processor as follows:

Port A	Mode 2
Port B	Mode Ø output
Port C (PC Ø, PC 1)	input

For further details, see the data sheet of the 8255A.

Control from the SPM-19 site:

The address 0 (A_8 = 0, A_9 = 0) is allocated to the sender from the receiver site. Decoding is carried out in IC 19/1 for data transmission receiver → sender and in IC 19/2 for the opposite direction. The data traffic is therefore controlled with the signals $\overline{PWR}$, $\overline{PRD}$, PA 8, and PA 9 from the receiver. The receiver fetches, with signal $\overline{PRD}$, data from IC 22, which is stored there by the processor of the PSS-19, or it writes, with signal $\overline{PWR}$, data into IC 22, which can then be read by the processor.

The traffic is coordinated with the signals $\overline{OBF}$ and $\overline{IBF}$ (see data sheet of 8255 for description). The signal $\overline{INTR}$ is controlled by software.

The signal 5 V_{cc} coming from the receiver is high only if the receiver is connected and switched on. If this is not the case, an interrupt RST 5.5 is initiated via IC 23/4 and IC 21/2, depending on the state of FF IC 23/2, IC 23/3.

An interrupt is also initiated when the receiver places a data byte in the 8255 (signal IBF = high).

The supply voltage in the PSS-19 can become > 0 V via the CMOS inputs and outputs of the data interface, although the PSS-19 is switched off. This means that the drivers of IC 22 on the interface side can assume an uncontrolled low impedance state. R 41 is fitted in order to keep the supply voltage sufficiently low in such cases.

The receiver can generate an interrupt (TRAP) in the PSS-19 via IC 19/2, using address 3 (PA_8 = 1, PA_9 = 1) *). This causes $\overline{IFC}$ to become low and the signal TRAP is generated via IC 32/1. (Note: IC 30/2 has an OC output).

9.2.1.7 Input and output ports

The I/O ports are standard circuits which are not described in more detail.

Input port	address C 4	IC 8/2, IC 26
Output port	address C 3	IC 27, IC 28
Output port	address C 2	IC 29
Output port	address C 1	IC 31

The other addresses decoded by the address decoder are used as software-controlled pulses. No ports in the normal sense are connected to these positions.

9.2.1.8 Battery voltage monitor

Shortly after the instrument has been switched on, C 2 still carries the voltage with which the RAM was supplied just before the power was switched on. This is compared with a reference voltage of 2.3 V (R 52, R 53) in IC 33 and the result is made accessible to the processor via IC 32/4 and IC 22.

*) (Interface clear for the IEC bus)

9.2.1.9 Power-on and power-off logic

Due to the use of the non-volatile RAM, special measures are necessary when the processor is started and when power is switched off.

As long as the instrument is switched off and, above all, during the periods where the supply voltage rises and falls, the RAM is protected against inadvertent accesses by the signal $\overline{\text{RESET IN}}$. R 48 ensures that $\overline{\text{RESET IN}}$ remains at a reliably low value even without a supply voltage connected.

When the instrument is switched on, the complementary flip-flop IC 34/2/IC 34/3 remains in the non-conducting state while the voltage rises. IC 34/1 therefore remains cut off and $\overline{\text{RESET IN}}$ remains low. This gives the following signals, with the signal POWER OFF[1] coming from the power supply unit:

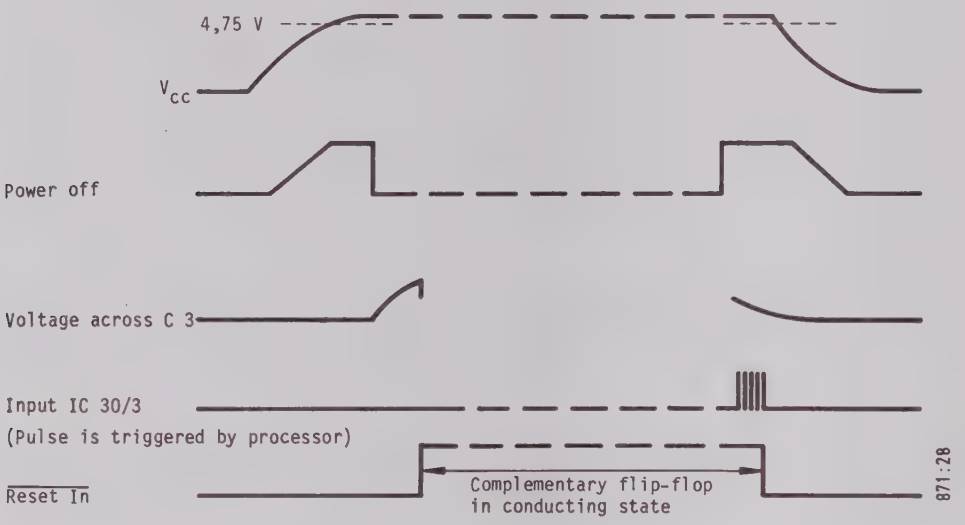


Figure 9-6 Power-on and power-off logic

Approximately 30 ms after the supply voltage reaches its nominal value, POWER OFF switches to low and the voltage across C 3 rises until IC 34/4 conducts. The complementary flip-flop therefore conducts and $\overline{\text{RESET IN}}$ goes to high. This simultaneously resets the processor and causes it to start executing the program. In this state, IC 34/4 conducts in the opposite direction. When the instrument is switches off, or if the power fails, the signal POWER OFF goes to high at least 2 ms before the supply voltage drops. As a result of this, an interrupt (TRAP) is triggered via IC 30/2 if flip-flop IC 32/1 / IC 32/2 is set. This flip-flop is reset by the software for a maximum of 1 ms only for the duration of short, uninterruptible program sections. At the end of the TRAP routine, the software generates pulses via IC 30/3 until the complementary flip-flop switches to the non-conducting state and the processor is stopped via $\overline{\text{RESET IN}}$.

The flip-flop will not switch to the off state with the first pulse only if the collector-base diode of IC 34/4 does not discharge capacitor C 3 sufficiently. It is thus immaterial whether 1 pulse or a maximum of approximately 50 pulses are required to change the state of the complementary flip-flop.

1) This signal is called "data retention" in newer documents.

9.2.1.10 Address decoding for front panel ports

IC 16/2 and IC 16/3 generate data strobes which are active only for front panel operations ($\overline{WF}$ and $\overline{RF}$). Decoding of the output ports of the level display is carried out with IC 38/1, IC 39/4 (injection of $\overline{WF}$), and IC 40. The single input port of the front panel is selected with IC 38/2, IC 39/2 and IC 39/1. IC 39/3 generates a selection signal for the output ports of the input circuit ($\overline{EWR}$). In this case, decoding of EA_8 to EA_{10} is carried out on the input circuit.

9.2.1.11 Contact bounce suppression circuit IC 35 to IC 37

The contact bounce suppression circuit used here is a so-called adaptive suppression circuit: the suppression time is increased to match the contact bounce time.

The signal ETG (pushbutton depressed) indicates whether a pushbutton in a valid column of the keyboard matrix has been depressed.

If no pushbutton is depressed, ETG = LOW. Counter IC 36/1 is therefore not reset (IC 37/4, IC 37/2) and is incremented until it reaches the value 8. At this point, Q 8 (pin 6) becomes HIGH and the count operation is terminated via pin 1 (clock). The other counter IC 36/2 is reset via IC 37/1.

When a pushbutton is depressed:

TG switches to HIGH. IC 36/2 is no longer reset and starts to run. As soon as a contact bounce pulse appears, the counter is temporarily reset. This reset operation is repeated until no contact bounce pulse has been received for approximately 22 ms, which means that the contact has closed completely. At the end of this 22 ms period, the counter has reached a value 8 ($Q_3 = 1$) and initiates the following operations:

- The count operation is stopped (pin 9 = clock becomes HIGH)
- IC 36/1 is reset via IC 37/4 and IC 37/2 because TG = HIGH.
- As a result of this, IC 36/2 can no longer be reset by contact bounce pulses, due to IC 37/3 and IC 37/1.
- IC 35 is set and triggers an interrupt in the processor.

This status remains stable until the pushbutton is released.

When a depressed pushbutton is released:

TG switches to LOW. IC 36/1 is no longer reset and starts to run. As soon as a contact bounce pulse appears, the counter is temporarily reset. This reset operation is repeated until no contact bounce pulses have been received for approximately 22 ms, which means that the contact is definitely open. The counter IC 36/1 has then reached the value 8 ($Q_3 = 1$). The circuit has now reached the state "no pushbutton depressed" (see above), and IC 36/2 is reset.

IC 35 is reset by software after detection of pushbutton operation.

9.2.2 INPUT CIRCUIT

9.2.2.1 Light emitting diodes

The LEDs are activated via drivers or decoders and via output ports IC 6, 8 and 10. If a decoder ensures that only one of a group of LEDs can be on at any one time, then a common series resistor is used for this group.

9.2.2.2 Keyboard matrix

The columns of the keyboard matrix are selected by the output port 40 (IC 2). The lines can be interrogated by the processor via input port 53 (IC 1).

In the idle state, all columns from which pushbutton operations can be accepted are set by software to LOW. The lines are all pulled to HIGH by IC 12, and the signal TG (pushbutton depressed) is LOW.

If a pushbutton in an active column is depressed, the corresponding line switches to LOW and the signal ETG switches to HIGH. An interrupt is now triggered in the processor by the contact bounce suppression circuit. The processor sets all columns except for one to HIGH and interrogates the lines via port 53. If all lines are HIGH, the pushbutton which was depressed is not in this column. The processor searches through all columns until the pushbutton which has been depressed is found.

If, in the idle state, a column is not set to LOW, i.e. not activated, then depression of a pushbutton in this column does not generate an interrupt. Depression of the pushbutton has no effect. The diodes Gl 1 to Gl 5 and resistors IC 12/7 and /8, together with R 7 to R 9, are required for the case where several pushbuttons in the same row could be depressed simultaneously. Without the diodes, the outputs of the column drivers would otherwise be short circuited together.

9.2.3 LEVEL DISPLAY (LED) (5)

The data placed by the CPU motherboard on the data bus (PEFD0...PEFD7)appear at the inputs of the latches (IC 4; 5; 7; 9; 10). The addresses PEA4B...PEA4F select the appropriate latches, which then accept the data intended for them. The clock supplied by IC 14 drives the counter (IC 1), which is incremented. The latches (IC 4; 5; 7; 9) in the corresponding digit drivers (IC 16; 17) are addressed via the decoder (IC 2). The outputs of the addressed latches switch from the tristate condition to the stored states, which causes 4 bits of information to pass to IC 6, where they are decoded and connected via the segment drivers (IC 19; T 1...T 7) to the internal "segment bus". The decimal point is activated via IC 8.

IC 11, 12, 13 decode the information for the dimensions written into IC 10. The special symbols ⇩; ⇧ and - and + are activated directly from the corresponding bits with the aid of the power circuits in IC 16; 18. The D/A converter constructed with IC 19 drives transistor T 9. This circuit section supplements the current so that a constant current is drawn by the complete circuit from the power supply unit.

Digit selection: Value of counter IC 1:				Selected latch	Selected digit
Q_4	Q_3	Q_2	Q_1		
L	L	L	L	IC 7,1	IC 29
L	L	L	H	IC 7,2	IC 28
L	L	H	L	IC 5,1	IC 27
L	L	H	H	IC 5,2	IC 26
L	H	L	L	IC 4,2	IC 25

9.2.4 APPENDIX

Port assignment lists

I/O ports in the PSS-19

Designation	Label/ Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ALC (Ref.-attenuator)										
Output-Attenuator	OUTATT C 1	0	1.)	20 dB #3 OAC	20 dB #2 OAC	20 dB #1 OAC	10 dB OAC	5 dB OAC	5 dB FAC	1.)
Ref.-Attenuator	REFATT C 3	0	Blanking	-4 dB	-2 dB	-1 dB	-0.8 dB	-0.4 dB	-0.2 dB	-0.1 dB
Control signals dBm corr. and generator off	STESIG C 2	0	1.)	ST 1	ST 2	Used by UBERPE!	Short time const.	1.) →		
				0	0	≙ 0 dB				
				0	1	≙ +0.03 dB				
				1	0	*) see below				
				1	1	≙ -0.04 dB				
Mixer:										
Carrier control	AUSGAN C 9	0 (J)	1.)	Signal on	Used by AUSGAN, see below !					
Output:										
Output selector switch	AUSGAN C 9	0 (I)	Used by T R A E S T ! see above		Rel 6 620 kHz 150 Ω	Rel 5 coax. 75 Ω	Rel 4 14 MHz bal. 124 Ω →	150 Ω	Rel 2 600 Ω ←	Rel 1 620 kHz bal. 0 Ω
Excess level +10 dB	STESIG C 2	0	1.)	Used by STESIG		Excess level +10 dB	1.) →			

*) Signal blank (digital blanking -20 dB) is not used by the software. This is provided for subsequent versions of the AGC amplifier for use as "20 Hz switching"

Figure 9-7 Control ports of the signal paths; port assignments

1.) Bits with this designation in output ports are not used.
Bits with this designation in input ports cause a "1" to be read.

2.) Bits with this designation in input ports can contain any information, which is explained elsewhere.

3.) Selection of this port (reading or writing or possibly both) causes the specified function to be executed; data as for 1.).

Designation	Label/ Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data (read and write)	Data C 8	IO	D a t a - B y t e							
Handshake signals	CA	I	$\overline{OBF}$	$\overline{INT}$ in SPM	IBF	Ø	Unde-fined	Free	2.)	2.)
Control words:										
Initialization request (mode 1)	CONTRO CB	0	1	0	1	1	1	0	0	1
Working mode (mode 2)			1	1	1	1	1	0	0	1
Reset interrupt (in mode 2)			0	1	1	1	1	1	0	1
Mode Ø			1	0	0	1	1	0	0	1
Interrupt SPM-V_{cc}:										
Enable	CC	IO	3.) →							
Disable	CØ	0	3.) only writing is possible							

Figure 9-8 Data interface to the SPM-19; port assignments

Designation	Label/ Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Programming switches										
Instrument matching and test	C4	I	Z_1 *) Switch No.: 1	Z_2 *) 2	Master reset *) 3	*) 4	Open = test, closed = operate 5	*) 6	1.)	2.)
Data maintenance:										
Check battery voltage of RAM	CA	I	2.) →						Voltage sufficient	2.)
Enable TRAP	CF	IO	3.) →							
Disable TRAP	CD	IO	3.) →							
Reset	CE	IO	3.) →							
TRAP-Status	CA	I	2.) →							Power off
Switches:										
dBm switch	C4	I	2.) →					1.)	1.)	0 ≙ dB 1 ≙ dBm

Figure 9-9 Soldered straps, data retention and switches on the rear; port assignments

*) Switch closed = 0 = active

The functions of the switches specified here are true only if S 5 is closed (in operation). In test mode (S 5 open) these switches are used for selecting the test programs.

Designation	Label/ Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Keyboard:										
Keyboard interr. reset	49	0	3.) →							
Columns	SPALTE 40	0	1.) →		5	Column 4	3	2	1	0
Rows	53	I	1.) →		Row 5	Row 4	Row 3	Row 2	Row 1	Row 0
LEDs:										
Output, Z values, etc.	TLD OUT 42	0	1.) →				See next sheet for definition O_3	O_2	O_1	$O_\emptyset$
Single LEDs (level)	TLD PEG 41	0	1.) →				See next sheet dB_1	$dB_\emptyset$	*) dBr 0	*) BLANK
LEDs REMOTE and AUTO BLANK	TLD BLA 43	0	1.) →			*) REMOTE	1.) →			*) AUTO BLANK

*) Ø = LED on, 1 = LED off

Figure 9-10 Keyboard and LEDs; port assignments

1.) Bits with this designation in output ports are not used.
Bits with this designation in input ports cause a "1" to be read.

2.) Bits with this designation in input ports can contain any information, which is explained elsewhere.

3.) Selection of this port (reading or writing or possibly both) causes the specified function to be executed; data as for 1.).

Output-LEDs:

O_3	O_2	O_1	$O_\emptyset$	LED-inscription
0	0	0	0	UNBAL 75 Ω
0	0	0	1	124 Ω — BAL I
0	0	1	0	150 Ω
0	0	1	1	150 Ω Z
0	1	0	0	150 Ω 0
0	1	0	1	600 Ω Z — BAL II
0	1	1	0	600 Ω 0
0	1	1	1	(All off)
1	X	X	X	

dB-LEDs:

dB_1	dB_0	LED-inscrption
0	0	dBr
0	1	dBm0
1	0	dBm
1	1	(All off)

Figure 9-11 1-out-of-n tables for LEDs (port assignments)

Column No. / Row No.	5	4	3	2	1	0
0	Decrement level, right digit (0.1 dB)	dBm0	1	8	/	/
1	Increment level, center digit (1 dB)	dBr	-	9	CLE	/
2	Decrement level, left digit (10 dB)	BLANK	3	6	AUTO BLANK	/
3	Increment level, right digit (0.1 dB)	dBm	0	7	dB dBm0	/
4	Increment level, left digit (10 dB)	Output ⇦ (Z_{out}-switching)	2	5	/	/
5	Decrement level, center digit (1 dB)	Output ⇨ (Z_{out}-) switching)	1	4	/	/

Figure 9-12 Keyboard matrix; (port assignments)

Designation	Label/ Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sign, decimal points, arrows, half digit	PEG VORTB 4E	0	1.)	DP 1 (First from right)	⇧	⇩	*) +	−	DP2 (second from right)	Half digit "1"
Digit 3 and digit 4	STE3U4 4D	0	Digit 4	B	C	D	Digit 3	B	C	D
Digit 1 and digit 2	STE1U2 4C	0	Digit 2	B	C	D	Digit 1	B	C	D
Dimension	PEGDIM 4B	0	See table below Di_7	Di_6	Di_5	Di_4	Di_3	Di_2	Di_1	Di_0

Dimension display

Display	Di_7	Di_6	Di_5	Di_4	Di_3	Di_2	Di_1	Di_0	in Hex
dB	0	0	0	0	0	0	0	1	Ø1
dBO	0	1	0	0	0	1	1	1	47
dBOp	0	1	0	1	0	1	1	1	57
dBr	0	0	0	0	0	1	0	0	Ø4
dBm	0	0	1	0	1	0	1	1	2B
dBmO	0	1	1	0	1	1	0	1	6D
dBmOp	0	1	1	1	1	1	0	1	7D
pWO **)	0	1	0	0	0	0	1	0	42
pWOp **)	0	1	0	1	0	0	1	0	52
Blank	0	0	0	0	1	1	1	1	ØF

*) minus sign must also be activated

**) DP3 appears simultaneously

Figure 9-13 Level display; port assignments

1.) Bits with this designation in output ports are not used.
Bits with this designation in input ports cause a "1" to be read.

2.) Bits with this designation in input ports can contain any information, which is explained elsewhere.

3.) Selection of this port (reading or writing or possibly both) causes the specified function to be executed; data as for 1.).

9.2.5 40 MHz OSCILLATOR AND PHASE-LOCKED LOOP (11)

Circuit diagram 871-7511.017

9.2.5.1 Introduction

The master frequency (40 MHz) is generated in an LC oscillator. This is coupled via a phase-locked loop to a precise and spectrally-pure reference frequency (10 MHz). For this reason, the quality of the signal is equivalent to the quality of the reference frequency.

In order to suppress harmonic frequencies, the oscillator is followed by a low-pass filter.

9.2.5.2 40 MHz oscillator

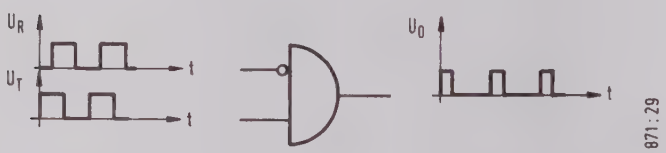
The LC oscillator is a Colpitts oscillator with the main components T 2, L 1, C 6, C 8, C 10-12 and Gl 3, 4. It is tuned by a phase-dependent DC voltage from a control amplifier. In order to linearize the capacitance-voltage characteristic of the diode, the control amplifier has a voltage-dependent load resistor (R 21, R 19, R 22, Gl 5). The signal current is extracted via T 1, which prevents retroactive effects.

It should be possible to blank the oscillator signal gradually. During this blanking operation, transistor T 4 takes over the current from T 1 in a virtually linear manner and conducts it to ground. The linearity as a function of time is achieved by means of the Miller effect, using capacitor C 13 and transistors T 4 and T 5.

9.2.5.3 Phase-locked loop

The DC-coupled buffer and amplification stage consisting of T 7 and T 8 drives the 4:1 divider (SN 74 S 74). The divided oscillator frequency is compared with the reference frequency in the phase discriminator consisting of T 11, T 13 and T 14.

The phase discriminator also acts as a limiter. It can therefore be regarded as a digital AND circuit with one inverting input.



The phase-dependent voltage is available at the collector of transistor T 11. This is smoothed with C 26 and freed of the reference frequency and its harmonics by the filter circuit between the emitters of transistors T 15 and T 16. This is followed by the control voltage amplifier T 16, via which the control voltage is connected with the correct level to the oscillator. The supply voltages are filtered additionally in the oscillator and phase-locked loop in order to prevent the power supply from affecting the amplitude and phase of the signals.

9.2.6 40 MHz LOW-PASS FILTER (12)

Circuit diagram 871-7512.016

This consists of a 9th order ∞ /1 Chebysev low-pass filter with a theoretical ripple of 0.18 dB. Its limit frequency is 44 MHz. The low-pass filter is supplied from the collector of the buffer stage in the oscillator and is terminated (150 Ω) by the mixer input.

9.2.7 LIMITER AND MIXER (13)

Circuit diagram 871-7513.015

The assembly "limiter and mixer" consists of the two printed circuit boards "limiter" [870-H] and "mixer" [870-G], which are mounted in separate screening boxes in order to provide good suppression of interference. The limiter board can operate alone, while the mixer board requires the bias voltage generated on the limiter board.

The carrier signal (40...65 MHz) passes through a high-pass filter (C 1, C 2, L 2, L 3) to a three-stage limiter and driver circuit consisting of IC 1 and T 3, T 4. Square wave signals of approximately 1 V_{pp} are available at the collectors of T 3 and T 4. Transistors T 1 and T 2 generate temperature-compensated bias voltages for the limiter and mixer.

The mixer is an active switching mixer in which the mixer transistors T 6, T 8, T 9, T 11 reverse the direction of the current generated by the current source transistors T 7, T 10 in the rhythm of the carrier signal. A low distortion master signal current of 40 MHz is superimposed on the currents through T 7 and T 10. The transformer O 1, together with the symmetrical circuit design, provide good suppression of common mode signals. The diode Gl 1 is a PIN diode which normally carries a direct current and has low resistance. If the master signal is blanked out, the direct current Gl 1 drops to zero, thus achieving a high blanking attenuation for the master signal.

9.2.8 25 MHz LOW-PASS FILTER (14)

The 25 MHz low-pass filter is a 9th order filter which is computer-approximated in accordance with the given masks.

The input and output impedances are $Z_{in} = Z_{out} = 150\ \Omega$. The main filter is preceded by an auxiliary low-pass filter in order to fulfil the high attenuation requirements up to 500 MHz.

The main filter is followed by an attenuator of 0.5 dB, followed by a further low-pass filter whose output capacitance is formed by a 9 cm long subminax cable (connection to next module). In order to achieve the high attenuation requirements, to avoid mutual coupling between the coils, and to guarantee a direct ground contact, the filter is installed in a 6 compartment case: the first compartment contains the auxiliary low-pass filter, the 2nd to 5th compartments the main filter, and the 6th compartment the attenuator and matching low-pass filter.

Repair or adjustment of this filter is possible only with restrictions.

9.2.9 AGC AMPLIFIER (15)

Introduction

The AGC amplifier is an amplitude control circuit, stabilized by a feedback loop, which has a bandwidth of 80 Hz to 25 MHz. At an input level of -25 dB, the circuit can generate an output level of +10 dBm to -74.9 dBm over the whole frequency range. The extremely precise output level and the flat frequency response result from the extremely precise 20 kHz reference level and precision, wideband attenuators. The control loop, with a high degree of negative feedback, operates with two switchable time constants. The normal time constant is used for frequencies above 10 kHz and reacts rapidly to changes of the input level. The longer time constant is used for frequencies less than 10 kHz.

The AGC amplifier not only offers high accuracy under normal operating conditions, but can also process swept input frequencies. In such cases, the circuit must not only react to changes in the input level, but must also compensate for the intrinsic frequency response of the signal path. For this reason, the signal path must have a very good frequency response over the whole bandwidth, independent of the automatic control.

Function and principle of operation

As can be seen from the block diagram, the module can be divided into 9 circuits. The RF section consists of the variable amplifier (1), output amplifier (2) and wideband attenuator (3). The negative feedback path consists of the loss-simulation circuit (4) and the follow-up rectifier (5). The reference signal for the data feedback loop is generated by the 20 kHz reference generator and passes through the precision reference divider (7). This signal is then fed to the follow-up rectifier (5). The regulation circuit (9) operates with the amplified differential voltage of the follow-up rectifier, generates the necessary loop gain, and thus determines the stability and the settling behavior of the control loop. The output voltage of the control circuit is fed to the variable amplifier, where the signal is attenuated as required. The last circuit is relay control circuit (8), which generates the control signals for the relay-switched attenuation stages in the wideband attenuator and for the loss-simulation circuit.

The input signal is fed to the variable amplifier, where it passes through the controlling element, an electronically-controlled attenuator. The output signal of this attenuator is amplified in a low-noise amplifier and then passed to the final amplifier for further amplification. At the output of the final amplifier, the signal is connected to two terminated outputs. The signal of the first output passes through the wideband attenuator to the output of the AGC amplifier. The second output of the final amplifier is connected to the loss-simulation circuit. This circuit precisely simulates the insertion loss of the output attenuator and the external impedance switching which follows the AGC amplifier. In addition to a fixed 5 dB attenuator, a 5 dB attenuator can be connected if levels greater than +5.0 dBm are required at the output.

The output signal of the loss-simulation circuit is connected, together with the reference signal coming from the reference divider, to two terminated RMS rectifiers. These rectifiers are designed such that equal input levels result in equal voltages at the outputs, regardless of the frequency of the signal connected from the final amplifier to the two halves of the rectifier. Each half of the rectifier generates a DC voltage which is proportional to the RMS value of the input signal. The two DC voltages are connected to a differential amplifier, amplified and passed on to the control circuit. Here, the control voltage is either amplified or attenuated as a function of the selected time constant. Phase correction elements provide the stability and the necessary settling behavior of the negative feedback loop. The output voltage of the control

circuit supplies the amplifier in the control element which, in turn, determines the attenuation of the control element. The negative feedback loop is thus closed.

For normal operation, the rectified signal from the loss-simulation circuit is compared with the rectified signal from the reference attenuator.

The amplified voltage difference generates a corresponding attenuation in the control element such that the output voltages of the two rectifiers become equal. Precise equality of the two rectifier halves indicates that the output level of the loss-simulation circuit has reached a value which is identical with that of the reference attenuator. As the frequency response of the loss-simulation circuit is also identical to that of the wideband attenuator and the external impedance switching, this means that the output signal is controlled precisely by the reference attenuator. As a result of this, the regulating effect of the negative feedback loop ensures that the output level of the instrument is precisely equal to that of the reference attenuator at any frequency within the operating range. However, this is not true if attenuator stages are inserted in the wideband attenuator or in the loss-simulation circuit.

Changes of the output level can be achieved in two ways: firstly, by changing the reference level with the reference attenuator and secondly by changing the attenuator settings of the wideband attenuator or feedback attenuator. The truth table shows all attenuator settings for various output levels. The reference attenuator provides an output level of 0 dBm to -4.9 dBm, which can be changed in steps of 0.1 dB. If it is assumed that the wideband attenuator is not connected in the circuit, and taking into account the fixed attenuation of 5 dB in the loss-simulation circuit, then the output level of the AGC amplifier varies between +5 dBm and +0.1 dBm when the output level of the reference attenuator varies between 0 and -4.9 dBm. The AGC amplifier is thus capable of generating an output level change of 4.9 dB in 0.1 dB steps, depending on the settings of the reference attenuator. As the truth table shows, the output attenuator can provide an attenuation of 75 dB in 5 dB steps.

The combination of reference attenuator and wideband attenuator generates a level of +5 dBm to -74.9 dBm, which can be varied in steps of 0.1 dB, at the output of the AGC amplifier. In order to generate an output level greater than +5 dBm, the switchable 5 dB attenuator in the loss-simulation circuit is activated. This causes the level at the final amplifier output to rise by 5 dB and permits, together with the range of the reference attenuator, level variation between +10 and +5 dBm.

As described above, the wideband attenuator and the fine steps of the reference attenuator generate an output level between +10 dBm and -74.9 dBm in steps of 0.1 dB. It should be noted that, when the 5 dB feedback attenuator is activated, a 5 dB gain step in the final amplifier is activated simultaneously in order to achieve the necessary increase of the output level.

As can be seen from the block diagram, the maximum gain of the signal amplifier stages is approximately 36 dB. For this reason, the attenuation of the control element must vary between approximately 10 and 15 dB, depending on the setting of the reference attenuator, at an input level of -25 dB. For variations of the input level of $\pm$3 dB, the control element must have a range of 7 to approximately 18 dB. In the position "blank generator", the output of the reference attenuator is blocked and a high control voltage is simultaneously injected into the control loop in order to set the attenuation of the control element to its maximum value of approximately 35 dB. The time constant, together with the blanking circuit, ensures that the signal is blanked and unblanked smoothly.

The control loop is equipped with two switchable time constants. In the normal operating mode, which is generally used for frequencies greater than 10 kHz, the bandwidth of the control loop is approximately 500 Hz. This provides rapid settling for changes in the input level and for changes in the reference attenuator setting.

In the operating mode "large time constant", the loop bandwidth is reduced drastically to approximately 17 Hz. This ensures that the signal to be controlled remains undistorted, which would not be the case if the control loop were to follow the instantaneous voltage variations. The time constant of the loop is switched at two points.

Firstly, the filter capacitance on the signal side of the follow-up rectifier is increased in the operating mode "large time constant". Secondly, the networks for magnitude and phase in the control loop circuit are modified. For the normal time constant, a further change is initated, namely connection of a high-pass filter with the limit frequency of approximately 1.6 kHz at the input of the final amplifier. This filter prevents a rapidly changing control voltage from acting through the control element, propagating itself in the signal path and leading to instability of the control loop.

The above sections describe the function of the AGC amplifier and the various sections of the circuit. In the following sections, the various circuits are described in more detail.

9.2.9.1 Variable amplifier (1)

The variable amplifier consists of two parts. The first is the control element, electronically-adjustable attenuator divider which acts as the variable attenuation element of the control loop. The control element utilizes the effect of the small signal resistance at the PN junction of a diode

$$r_d = \frac{nkT}{q \cdot I} \approx \frac{40}{I\ (mA)} \quad \text{Ohm}$$

In this the AC impedance is inversely proportional to the applied current I. The voltage divider consists of a network of such diodes. The series path consists of diodes Gl 3 to Gl 10 and capacitors C 3, C 4, C 7, C 6 and C 8, together with resistor R 9 and inductance L 3. C 29 divides the input signal equally between the two halves of the series path at high frequencies. The parallel path consists of diodes Gl 11 to Gl 14 and Gl 16 to Gl 19 and capacitors C 9 and C 11. Each path of the divider consists of 4 diodes in series, to which a further 4 diodes in series are connected in parallel, but in the opposite direction. The resulting impedance of each path can therefore be represented as follows:

$$R_d \approx \frac{80}{I\ (mA)} \quad \text{Ohm}$$

It should be noted that all 8 diodes in each path are connected in series if they are regarded as a DC circuit. For this reason, all diodes present the small signal resistance. In contrast to this, regarded from the point of view of the signal flow, each path consists of 4 series diodes connected parallel to 4 series diodes with opposite polarity. The symmetry of this arrangement ensures that distortion products caused by signal currents, which are superimposed on the controlling DC signal, are negligible. The symmetry also reduces the distortions resulting from non-harmonic components. Furthermore, the distortion of harmonic components is reduced more by 4 series junctions than by one. At the same time, the signal voltage drop across each diode is reduced. The attenuation of the attenuator increases as the control voltage increases, as the direct current in the parallel diode path increases while the direct current in the series path decreases.

The control current for each path of the control element is generated by a symmetrical voltage, which is connected to the current-limiting resistors of each half of the diode arrangement. This results in a high degree of symmetry in each diode row and prevents variations of the control voltage from being propagated through the signal path, as this could endanger the possibility of the control loop. The control voltage is connected to an amplifier consisting of IC 1/3 and IC 1/4 which generates the symmetrical voltages. This supplies the parallel path of the control element and an inverter IC 1/1, which supplies the series path of the control element. In the parallel path of the control element, there is an inverting amplifier IC 1/3 which generates a voltage with precisely the same magnitude but the opposite polarity to that generated by the non -inverting IC 1/4. In this manner, voltages of the same magnitude but opposite polarities are connected via resistors R 15 and R 16 to the diode network. In the parallel path of the control element, it is necessary to increase the current considerably if a high attenuation is required. This is achieved with transistors T 3 and T 4, which increase the diode bias current in the parallel circuit in the case of a high control voltage.

The series path of the control element is supplied by IC 1/2 and the inverting IC 1/1. The inverting amplifier inverts the control voltage and generates a voltage offset with the aid of the network R 2, R 3, and Gl 21. The diode Gl 21 provides a temperature-dependent offset voltage which compensates for the temperature coefficient of the control element. This type of compensation provides a stable ratio of the currents in the series and in parallel paths over the whole operating temperature range. The inverting amplifier IC 1/1 which supplies the series path has a DC gain of 2.3. This increases the sensitivity of the series path of the control element and simultaneously provides a constant loop gain over the whole attenuation range of the control element. In addition, the gain of the IC 1/1 is increased by R 35, C 27 and C 28 and high control loop frequencies. This gain increase compensates for the reduced sensitivity of the rectifier at low levels, to which reference will be made later.

R 39 and R 40 are current-limiting resistors which ensure that IC 1/1 and IC 1/4 are overdriven before IC 1/2 and IC 1/3. As the two latter ICs are inverting amplifiers fed by IC 1/1 and IC 1/4, they precisely simulate the form of the overdrive signal. This ensures that the control voltages for the series and parallel paths remain symmetrical even at high overdrive levels.

Resistor R 9 and coil L 3 represent the minimum impedance of the series path of the control element and thus determine its maximum attenuation. L 3 is a frequency-compensation element which compensates for the inductive component of the diodes in the parallel paths at high attenuations. The input impedance of the control element is approximately 110 Ω over the whole operating range. Resistor R 36 is used to increase this impedance to approximately 150 Ω.

As described in the previous sections, the control element generates an insertion loss for the applied signal which is approximately proportional to the connected control voltage. The output signal of the control element passes through the low-noise preamplifier, the second stage of the variable amplifier.

The low-noise preamplifier is a two-stage negative feedback amplifier consisting of T 1 and T 2. The gain of this wide-band amplifier is determined by R 22 and R 23 and is approximately 18 dB from 80 Hz to 25 MHz. The flat frequency response is achieved by shifting the phase of the negative feedback signal with the aid of a network consisting of C 15, C 16 and R 26. The components R 38 and C 24 provide gain correction at low frequencies. This is intended to compensate for the increased input load of the control element caused by R 6, R 7, C 2 and R 10, R 11 and C 5. R 30 determines the output impedance of the amplifier. When the amplifier is terminated, its gain is 12 dB.

As described above, the combination of control element and preamplifier guarantees a uniform voltage level over the frequency range 80 Hz to 25 MHz. The control element has a flat frequency response over its attenuation range of 7 to 18 dB. The output of the variable amplifier drives the output amplifier.

9.2.9.2 Output amplifier (2)

The final amplifier is a three-stage, wideband, negative feedback amplifier, whose output drives a complementary emitter follower stage which has two separate but identical outputs, each with an output impedance of 75 Ω. The gain of this amplifier is approximately 19 dB between 80 Hz and 25 MHz. The gain of the negative feedback amplifier consisting of T 1 to T 4 is determined by resistors R 12, R 13 and R 17 together with R 10. This type of negative feedback results in a parallel-series negative feedback amplifier. Additional frequency emphasis is achieved with components R 11, C 8, C 9, R 50 and C 44. This frequency emphasis network is intended primarily to compensate for the insertion loss of the output attenuator. At the same time, it results in a flat frequency response from the input to the output of the AGC amplifier, even if the control loop is open.

An additional gain of 5 dB is achieved by increasing the input impedance, this being switched with Rel 1. As described above, this gain increase is activated together with the 5 dB attenuator in the negative feedback attenuator. The AGC amplifier thus has an additional gain which is necessary at high output levels.

In the operating mode "normal time constant", a high-pass filter with a limit frequency of approximately 1.6 kHz is formed by the coupling capacitors C 39 and C 45. These oppose the input impedance of the negative feedback amplifier. If the operating mode "large time constant" is selected, the relay (Rel 2) for the loop speed is activated, and connects C 5 into the circuit. This shifts the lower limit frequency towards 80 Hz. At the same time, another relay contact closes a connection through L 9 and L 8 to the rectifier circuit. This increases the time constant of the rectifier in a manner which will become clear in the following description of the circuit.

The output of the negative feedback amplifier drives a complementary emitter follower stage T 5 and T 6, which has two separate outputs, each with an impedance of 75 Ω. The reflection coefficient of each output is improved by RC circuits consisting of R 47, C 35, C 31 and R 48, C 37, C 32. Output A drives the negative feedback loop via the loss-simulation circuit, while output B drives the output attenuator stage.

As described above, the output amplifier has a gain of approximately 19 dB. Two highly-decoupled outputs for the output attenuator and the negative feedback loop are provided. Together with the variable amplifier, the overall frequency response is flat, in the operating mode "large time constant" from 80 Hz to 25 MHz and in the operating mode "normal time constant" from 10 kHz to 25 MHz. Correction elements in the output amplifier provide emphasis in order to compensate for the insertion loss of the following output attenuator. Attention was paid to a flat frequency response from the input to the output over the whole operating frequency range.

9.2.9.3 Wideband attenuator (3)

The wideband attenuator is a precision attenuator whose switchable attenuator stages cover a range of 0 to 75 dB in 5 dB steps. It consists of 5 stages: three 20 dB attenuators, one 10 dB attenuator and one 5 dB attenuator. Each divider stage consists of one or two π elements, which are constructed with highly-stable metal film resistors. Each attenuator is switched on or off by a miniature relay. Each attenuator contains elements for frequency compensation which are fitted during final testing in order to optimize the frequency response of each separate attenuator.

The insertion loss of the wideband attenuator results on the one hand from the contact resistance of the relays (which increases with the frequency) and on the other hand from the reactances which are distributed throughout this circuit. The increased resistance of the relay contacts is caused by the skin effect in the ferrous metals used in the relay. For this reason, the characteristic impedance at the inputs and outputs of the attenuators tend to increase with the frequency. This effect is virtually compensated by addition of RC circuits, which are inserted at the connection points of the attenuators. The purpose of these circuits is to reestablish the impedance of 75 Ω at the connecting points between the various attenuators. The correction elements which optimize the reflection factor of the attenuator consist of R 1 and C 1 at the input, of R 17 and C 5 in the third attenuator, of R 25 and R 7 in the fourth attenuator and of R 30 and C 9 in the fifth attenuator. The values of some of these RC circuits are modified during alignment. They ensure that a satisfactory reflection coefficient of the complete structure is maintained even if the relays are not activated.

An additional correction of the reflection coefficient is carried out at the outputs of the first 20 dB attenuator, of the 10 dB attenuator and of the 5 dB attenuator. These correction elements, consisting of C 17, C 18, C 20, C 21 and C 22, C 23, provide a satisfactory reflection coefficient at all combinations of the attenuators.

Additional correction circuits for the frequency response are used in the three 20 dB attenuators and in the 10 dB attenuator. These circuits consist of R 36, C 25 and C 14, R 37, C 26 and C 15, R 38, C 27 and C 16 and R 39, C 28 and C 19. These elements are adjusted during final alignment of the instrument in order to achieve an optimum frequency response for each attenuator.

As described above, the wideband attenuator can generate an attenuation of 0 to 75 dB in 5 dB steps over the whole frequency range. Extremely precise π networks, supported by compensation elements for return and insertion loss, ensure very precise attenuation of the output signal on the AGC amplifier.

9.2.9.4 Relay control (8)

The relay control circuit converts the 5 V positive logic signals into 12 V switching signals in order to activate the relays in the AGC amplifier. In addition to the 5 relays in the wideband attenuator, this circuit controls the 5 dB negative feedback attenuator in the loss-simulation circuit and the 5 dB gain relay in the output amplifier. It also contains the control for the switch for the two time constants, which is also located in the output amplifier. As can be seen from the circuit diagram, two parallel drivers are used for the 5 dB switch in the negative feedback circuit, as the 5 V gain switch in the final amplifier is operated in parallel to this. In addition to voltage transformation of the logical signals for driving the relays, this circuit is also used to isolate the relays from the selection circuit, and thus to reduce the possibility of crosstalk between the relays via the selection circuit.

9.2.9.5 Loss-simulation circuit (4)

The most important function of the loss-simulation circuit, as its name indicates, is to generate an insertion loss with the frequency response which is practically identical to the insertion loss of the wideband attenuator and the external output circuit. The negative feedback loop therefore generates a signal which is slightly raised for the frequency response at the output of the wideband amplifier, in order to provide a signal with a flat frequency response at the output socket. In addition, the loss-simulation circuit contains one fixed and one switchable 5 dB attenuator. The frequency response of the insertion loss of the wideband attenuator consists of an extremely complex function. This almost completely compensates for the insertion loss of the relays. This insertion loss is due mainly to the skin effect in the ferrous materials used in the relays. This attenuation, which is equal to the square root of the frequency curve, is extremely difficult to simulate with discrete components. In the loss-simulation circuit, a coil consisting of a piece of iron wire similar to that used for the relay connections is used. This element has its maximum effect in the frequency range from approximately 100 kHz to approximately 10 MHz. The circuit provides space for pieces of wire which can be added during final alignment in order to compensate for the insertion loss of the wideband attenuator in this frequency range.

A further important factor which contributes to the insertion loss of the wideband attenuator is the three RC circuits in the 5 dB, 10 dB and first 20 dB attenuator. The attenuation caused by these circuits is compensated in the loss-simulation circuit with R 7, C 5 and C 6. R 12 and C 10 optimize the reflection factor at the input of the loss-simulation circuit. The RC circuit consisting of R 6, C 13, C 4 and the variable capacitors C 9 is used during alignment of the rectifier unit to provide a flat frequency response with the control loop closed.

A fixed 5 dB attenuator consisting of R 8, R 9, R 10 and R 11 separates the follow-up rectifier from the impedance of the equalizer.

The 5 dB negative feedback attenuator is a π circuit and is constructed with precise metal film resistors. The RC circuit R 2, C 3 and the resonance circuit L 3 and C 11 provide adjustment facilities for the frequency response when the 5 dB attenuator is active.

The resonance circuits in the loss-simulation circuit have resonance frequencies which lie above 160 MHz. They are necessary to compensate for the internal impedances of the loss-simulation circuit.

As can be seen from the circuit diagram, many of the compensation elements are variable and can be adjusted during final inspection. This is necessary because the insertion loss of the wideband attenuator varies from one circuit to another. For this reason, the loss-simulation circuit is "married" in final inspection with a specific wide-band attenuator. This high flexibility in adjustment of the loss-simulation circuit and the extremely flat frequency response of the follow-up rectifier are responsible for the high performance of the AGC amplifier.

9.2.9.6 Rectifier (5)

The rectifier is the heart of the AGC amplifier. It consists, essentially, of two identical rectifiers. These process two signals, which come from the loss-simulation circuit and the reference attenuator. The filtered DC signals from the two rectifiers are fed to a differential amplifier which passes a highly-amplified difference signal to the control loop. A forward control circuit senses variations of the reference input level and passes a DC compensation voltage to the coupling capacitors at the input of the signal path and to the capacitor in the loop filter for large time constant. This ensures that the capacitors can reach their final charge rapidly. The forward control circuit drastically reduces the settling time of the AGC amplifiers after changes in the reference attenuator.

As can be seen in the circuit diagram, the rectifier consists of the double transistors T 1 and T 2, which are connected as diodes, and which are operated with a bias current of approximately 2 mA. The double transistors are selected for identical DC voltage temperature coefficients. Each half of the rectifier consists of two selected transistors with the same temperature coefficient. This achieves a high DC stability between the two rectifiers. Both signals, from the signal input and the reference input, which vary nominally between 0 and -4.9 dBm, are attenuated by approximately 14 dB before being connected to the diodes of the rectifier. The attenuators consist of R 7, R 6 and R 8 on the reference side and R 15, R 13, R 14 together with R 22 on the signal side. The frequency response for varying levels can be adjusted with C 13.

The output of the reference half of the reference rectifier is filtered with C 7. In the same manner, the output of the signal-half is filtered with C 16 and C 9. In the case of the operating mode "large time constant", C 8 is connected in order to increase the time constant by a factor of 11. Switching is carried out by the fast-slow relay in the final amplifier as described above. The filtered DC voltage signals of the two rectifier halves are connected via R 4 and R 3 to IC 1, a differential amplifier with a high gain. The gain of this differential amplifier, which is very high for DC voltages, drops by 6 dB per octave due to C 2 and C 3, and flattens out at 20 dB due to resistor R 2. This reversal frequency contributes primarily to the time constant in the control loop, as do C 9 and, in the operating mode "large time constant", C 9 plus C 8. The control voltage at the output of IC 1 is the highly-amplified differential voltage which exists between the two halves of the rectifier. This difference voltage is held at 0 V by the control loop when the circuit has settled.

A change in the reference input level results in a change of the DC voltage across C 7 and C 4. This voltage change causes, due to the loop gain of the control loop, a change in the level of the input signal. The resulting voltage across C 9 is equal to that across C 4. More important, however, is the fact that a DC voltage change corresponding to half the value across C 9 would be necessary in order to cause the same effect via the input coupling capacitors C 10, C 11 and C 12 at the signal input. The large time constant, together with these capacitors, would seriously increase the settling time of the control loop after changes in the reference level. In order to compensate for these voltage changes, the forward regulator consisting of IC 2/2 generates an input voltage change across resistor R 14 which is precisely equal to that necessary for the settled state. For this reason, no voltage change across the input coupling capacitors is necessary, and the settling time is not increased.

In the same manner, it will be necessary in the operating mode "large time constant" to match the voltage across C 8 to that across C 4. Due to the large time constant, this would drastically increase the settling time of the loop after changes of the reference level. In this case, the forward regulator generates a voltage step referred to the AC ground and parallel to C 8 via the fast-slow relay in the output amplifier. In this manner, the voltage across C 8 in the settled state does not change when the reference level changes. The settling behavior is improved. The rectifier is sensitive to noise from the supply voltage. In order to guarantee extremely low noise supply voltages, the positive and negative voltages are connected via active decoupling circuits. For the positive supply voltage, the decoupling circuit is located in the reference generator; for the negative voltage, it is in the control circuit. These active decoupling circuits supply the rectifier with $\pm$11.3 V.

As described above, the rectifier operates with selected pairs of rectifiers which process the reference voltage and the signal voltage. The resulting DC voltages are connected to a differential amplifier, and the amplified difference signal is connected to the control circuit.

9.2.9.7 Control circuit (9)

The control circuit generates a frequency-dependent correction of the control voltage in its magnitude and phase. It operates with the aid of the fast-slow control signal. The control circuit also includes the output blanking function, which uses a clamping circuit which generates the maximum possible control voltage and thus the maximum attenuation of the signal path. Furthermore, the circuit contains the active decoupling element for the negative supply voltage of -11.3 V for the rectifier.

The input signal of the control loop comes from the differential amplifier of the rectifier. In the operating mode "normal time constant" (fast), this signal passes via low-pass filter R 21 and C 9 to IC 1/1. In the fast operating mode, this amplifier has a DC gain of approximately 21 dB, determined by R 14 and R 16. As the frequency of the control voltage increases, the gain is increased with components R 15, C 12 and C 6 to its maximum value of approximately 33 dB. This network and the gain correction over the frequency provide the necessary phase correction in the transition of range. The output of IC 1/1 generates the control voltage via R 12 for the variable amplifier. R 12 is a plug-in resistor which permits the control loop to be opened for fault-finding purposes. A wave trap consisting of C 3, C 4 and L 1 is fitted at the control voltage output. This suppreses the 20 kHz from the reference generator. The diode, Gl 3, is also connected at the output to prevent the control voltage from reaching high negative values during settling.

The low-pass filter at the input, consisting of R 21 and C 9, has a limit frequency of approximately 9 kHz. This reduces the noise modulation on the high frequency signal which is generated in the control loop. The RC combination consisting of R 17, R 18 and C 5 provides a decoupled bias voltage at the input of IC 1/1 which suppresses unwanted overshoot during switching between the operating modes "large time constant" and "normal time constant".

In the operating mode "large time constant", the fast-slow control signal actuates two switches in IC 2. The first switch bypasses the negative feedback network of IC 1/1 and converts this into a linear voltage amplifier. The second switch connects capacitors C 7 and C 8 of the input circuit to ground. The resulting network at the input of IC 1/1 is now R 20, C 7, R 19 and C 8. This represents a second order low-pass filter which reduces the loop gain at very low frequencies when the large time constant is selected. In the operating mode "normal time constant", in which IC 2 is not active, C 8 is connected in series with C 7 and bypasses R 19, and therefore has a negligible effect. In both operating modes, the frequency-dependent gain, which is injected into the control loop by the control circuit, cooperates with other frequency-dependent components within the variable amplifier and the rectifier. These three circuits determine the overall negative feedback behavior and thus the settling behavior and loop stability of the AGC amplifier.

The second important function of the control circuit is the blanking function. If a logical 5 V signal is connected to the blanking input, it is connected via R 1, R 2 and the filter capacitor C 1 to the DC reference input of the rectifier. A voltage at the reference input rising positively causes the control voltage to rise rapidly and results in high attenuation of the high frequency. An active clamping circuit consisting of IC 1/2 monitors the control voltage and reduces the voltage connected to the reference input via R 4 and Gl 6, holding the control voltage at approximately 4.8 V. This results in maximum attenuation in the high frequency path. The blanking signal is connected at the same time to the reference attenuator, causing the reference signal at the input of the rectifier to be reduced. The combination of both operations results, in the control element, in an attenuation of at least 35 dB over the whole frequency band.

The control loop also has an input for an external reference voltage, which is connected via R 3 to the reference input of the rectifier. It should be noted, under these conditions, that the reference attenuator is set to maximum attenuation and the reference signal is determined exclusively by the externally-connected signal in the rectifier.

An auxiliary circuit in the control circuit is the active decoupling element T 2 for the rectifier. The - 11.3 V generated here is strongly decoupled from the noise of the power supply unit and residual ripple from mains rectification.

As described above, the control circuit ensures that the negative feedback operates with a controlled frequency response and thus guarantees loop stability and best possible settling. In addition, the circuit contains the blanking function and limits the control voltage to a value between -0.7 and +4.8 V. This ensures that the control circuit always operates in its linear range.

9.2.9.8 Reference generator (6)

The reference generator generates a 20 kHz frequency with a stable level which is connected to the reference attenuator and then as the reference signal to the rectifier. The reference generator also contains the active decoupling of the positive supply voltage for the rectifier.

The reference generator is a Wien bridge oscillator consisting of IC 1 and the frequency-determining components R 1, C 1, R 2 and C 2. It is a well-known fact that a Wien bridge oscillator requires a voltage gain of precisely 3 in order to maintain its oscillation. The voltage gain of IC 1 is determined by R 5, R 3, R 4 together with the variable resistor represented by the field-effect transistor T 1. The output amplitude of the reference generator is regulated by the control loop consisting of the peak rectifier IC 2/1, transistor T 2, filter capacitor C 7 and field-effect transistor T 1. IC 2/2 has a bias voltage in order to generate the maximum negative voltage of which the IC is capable at its output. This voltage is thus closely matched to the maximum negative output sweep of IC 2/1. This, in turn, generates a temperature-compensated emitter voltage for transistor T 2 and effectively eliminates changes due to temperature as the result of voltage changes at the emitter of T 2. T 2 is normally cut off and conducts only when the voltage at the inverting input of IC 2/1 exceeds -8.4 V. This occurs during extremely short current pulses through transistor T 2, which charge C 7 to a value between -1.8 and -3.2 V. This voltage is connected to the gate of T 1. The higher this negative voltage becomes, the higher is the resistance of T 1, and the higher R 3 and R 4 lie above ground. The variable resistance of T 1 maintains the voltage gain of the oscillator at precisely 3 and thus maintains the sinusoidal oscillation. The amplitude of the output signal is held at a nominal peak voltage of -8.4 V, depending on the precise value of the reference diode Gl 1. The output signal drives the reference attenuator via P 7 and R 8. The amplitude control loop has a long time constant determined by R 11 and C 7. Resistor R 16 damps settling oscillations which result when the supply voltage is connected to the circuit.

The decoupled +11.3 V supply voltage for the rectifier is generated by transistor T 3. This is a voltage with an extremely low noise value, free of noise from the voltage supply and from mains frequency components.

As described above, the reference generator provides a highly stable 20 kHz signal with a peak value which is determined by a very stable reference diode. This voltage is connected via a resistance network, which permits adjustment of the level over a very small range, into the reference attenuator. The output signal current is adjusted such that it delivers a maximum level of 0 dBm to the reference attenuator.

9.2.9.9 Reference attenuator (7)

The reference attenuator processes the signal from the reference generator. It provides precise attenuation in 0.1 dB steps between 0 dB and -7.9 dB. The output level of the reference attenuator is a signal in precise steps between 0 and -4.9 dBm, as 3 dB of the range are not used. The attenuator also has a blanking position which completely suppresses the output signal. In addition, small gain corrections of +0.03 dB (correction No. 1) and -0.04 dB (correction No. 2) are possible and can be superimposed on the setting of the attenuator.

The reference attenuator consists of three attenuator chains. Each of these can be switched by means of 8 x 1 semiconductor switches. Each attenuator chain is separated from the others by operational amplifiers acting as buffers. The input current from the reference generator is connected to amplifier IC 1/1, which presents a virtual ground for the reference generator. This means that the output voltge of IC 1/1 is determined by R 3 together with the output impedances of the reference generator. This voltage is approximately 0.55 V RMS. The output of IC 1/1 is connected to the first attenuator chain, whose output is selected by multiplexer IC 3. The selected output of IC 3 is connected through operational amplifier IC 1/2 to the second divider chain, whose output is selected with IC 4. The voltage selected with IC 4 is connected to operational amplifier IC 2/1, whose output signal passes to the third attenuator chain which is switched with IC 5. The output signal passes through the buffer amplifier IC 2/2 and resistor R 41 to the ouput of the reference attenuator. R 41 represents a 75 Ω source impedance for the reference input of the rectiifier. Transistor T 1 increases the current gain of IC 1/2 in order to guarantee an undistorted output signal.

Attenuation in the reference attenuator is carried out in three steps, as described above. The third attenuator chain, selected by IC 5, attenuates in 0.1 dB steps between 0 dB and 7 dB, corresponding to the BCD signals at pins a4, a2 and a3. The second attenuator chain, selected by IC 4, provides attenuator steps of 0 dB, 0.8 dB, 1 dB, 1.8 dB, 2 dB, 2.8 dB, 3 dB and 3.8 dB, corresponding to the logical signals at connection pins a7, a12 and a11. Finally, the first attenuator chain, selected by IC 3, provides large attenuator steps and the small correction values. This attenuator chain generates steps of +0.03 dB, -0.04 dB, -3.97 dB, -4.0 dB and -4.04 dB. Two other attenuator steps of approximately -20 dB or -24 dB can be connected into the circuit in accordance with the logical signals at pins a10, a9, a8.

The three attenuator chains together cover the normal attenuator range of 0 dB to 4.9 dB in 0.1 dB steps. Small attenuation corrections of -0.04 and +0.03 dB can be superimposed on this range. The reference attenuator also provides an additional attenuation of 20 dB. Normally, this step is used with the blanking function. Its accuracy is reduced and does not include the small correction factors.

Blanking of the reference generator is carried out via IC 5 with the blanking signal at pin a6. When the blanking signal is present, the output level of the reference generator is completely blocked. As described above, this, together with blanking of the control circuit, provides the maximum attenuation in the high frequency path.

As described above, the reference attenuator, which processes the signal from the reference generator, provides a precisely-controlled output level between 0 dBm and -4.9 dBm and passes this signal to the reference input of the rectifier. In addition, this signal can be attenuated via a further 20 dB or completely blocked by means of the blanking input.

9.2.9.10 Negative feedback loop

The negative feedback loop is an extremely complex, non-linear circuit whose characteristics can be described only approximately over a small working range.

Two special non-linear elements are used in the control loop. The first is the rectifier, which operates as an RMS detector. It has a high sensitivity as a function of the input level. At an output level of 0 dBm, the rectifier has a sensitivity of approximately 250 µV for a level change of 0.01 dB. At an output level of -4.9 dBm, the sensitivity is approximately only 80 µV for a level change of 0.01 dB. The rectifier sensitivity varies by approximately 10 dB over the normal working range of the rectifier. This varying sensitivity explains the characteristic curve of the control loop.

The second important non-linear element is the sensitivity of the control element as a function of the required attenuation. If it is remembered that the impedance of the control element diodes varies inversely with the injected current, then it is apparent that the attenuation sensitivity of the control element is directly dependent on the working point. Either the series or the parallel path reduces its sensitivity as the current increases, and the sensitivity increases when the current drops.

In the control element, these two effects virtually counteract each other. Whereas the sensitivity in the parallel path drops, the control current rises. At the same time, the sensitivity in the series path rises and the current drops. Over the working range of the control element, the sensitivity thus remains sufficiently constant.

The limit frequency of the control element, regarded from the control loop point of view, is determined by the parallel path consisting of R 15, R 16, C 9, C 11 and the instantaneous impedance of the voltage divider of the parallel diodes. At an output level of 0 dBm, the nominal current in the series and parallel paths is approximately 0.5 mA. Under these circumstances, the limit frequency of the parallel path is approximately 29 Hz. This is much lower than that of the series path, and is thus dominant in the frequency behavior of the control element with the control loop open. It is important to note that the limit frequency varies as a function of the control voltage. However, this behavior is accompanied by a change in the sensitivity such that the sensitivity of the parallel path drops as the limit frequency rises. This means that the change in sensitivity is unimportant for frequencies above the limit frequency of the control element.

Under these circumstances, the sensitivity of the control element can, as a first approximation, be regarded as linear with a single, simple pole at approximately 29 Hz. For the following sections, it should be remembered that this is an approximation and that the actual circumstances are to a high degree non-linear and deviate considerably from this ideal representation. Nevertheless, this is sufficiently accurate in order to determine the settling behavior and the stability of the control loop.

As mentioned above, the rectifier's sensitivity varies by 10 dB over its operating range. In order to understand the function, it is necessary to know that the sensitivity drops slowly as the output level of the reference attenuator decreases and, as a result, requires an increase in the attenuation of the control element. This increase, as mentioned above, is determined primarily by the behavior of the series path of the voltage divider. In order to compensate for the reduction in the sensitivity of the rectifier, the gain of the drive circuit in the series path is increased. This is achieved by components R 35, C 27, C 28.

This combination causes a gain increase, starting at approximately 10 Hz and ending at approximately 30 Hz, for the series path of the control element. This gain increase compensates for the reduced sensitivity of the rectifier at low levels.

The loop gain is dimensioned such that the stability is guaranteed over the whole control range and that the settling behavior has only a slight tendency to overshoot.

With the fast time constant, the loop gain passes through 0 dB at 400 Hz. In the slow mode (large time constant), the loop gain passes through 0 dB at 17 Hz.

9.2.10 OUTPUT SECTION (16)

See circuit diagram 871-7516.012

9.2.10.1 Overall function of the output section

The task of the output section is to connect the 75 Ω output of the AGC amplifier to one of the three instrument outputs. Due to the relay logic used, it is possible to obtain a single signal at only one output, and not at several outputs simultaneously.

Three possible outputs are:

1) Output UNBAL: unbalanced, 80 Hz ... 25 MHz, Z_{out} = 75 Ω
2) Output BAL I: balanced, 60 kHz ... 14 MHz, Z_{out} = 124/150 Ω
3) Output BAL II: balanced, 80 Hz ... 620 kHz, Z_{out} = 0/150/600 Ω
   (See block diagram of output section)

For the output UNBAL, the signal of the AGC amplifier is switched through directly without frequency response corrections, as the control loop of the AGC amplifier includes simulation of the frequency response of the connection cable, of the switching relay, and of the other connection components, which means that these losses are compensated in the control element of the AGC amplifier and are thus compensated as far as the output. For output BAL I, the signal of the AGC amplifier passes through a balancing transformer. This carries out balancing conversion to Z_{out} = 124 Ω or Z_{out} = 150 Ω.

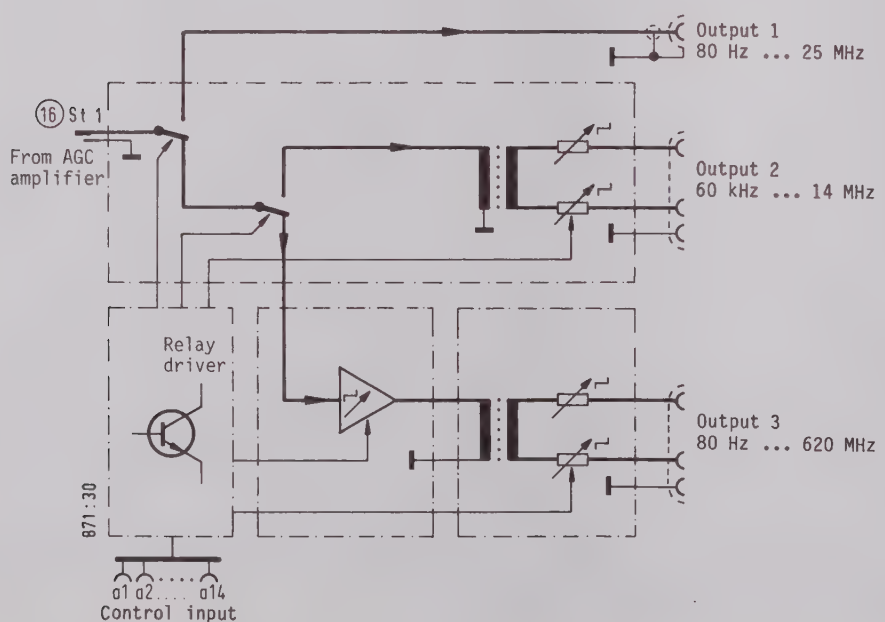


Figure 9-14 Block diagram of output section

The signal path for the output BAL II contains, in addition to a balancing transformer, an buffer amplifier which permits selection of output impedance Z_{out} = 0 and an additional excess level of "10 dB". The input impedance of the buffer amplifier is 1 kΩ.

9.2.10.2 Board "output 2"

(See circuit diagram)

The board "output 2" carries, in addition to the balancing transformer for output BAL I, the switching of the input signal to the various outputs (Rel. 5 and Rel. 4).

As two relays with their contacts connected in series are used, only one output can be active even if the drive to the circuit is incorrect.

This board also implements direct connection of the output UNBAL. In order to achieve the best possible transmission characteristics, the wiring on the printed circuit board is in the form of 75 Ω strip conductors.

In order to avoid level losses, transformer Ü 1 should act as a transformer for power levels, i.e. it should transform the 75 Ω source impedance of the AGC amplifier into the required value of 124 Ω or 150 Ω. However, as the transformer can be wound only with integral numbers of turns, the required theoretical conversion ratio cannot be obtained precisely. In addition, it is necessary to transform to two different impedances. For implementation, the intregral conversion ratio which transforms close to, but below, the required value of 124 Ω has been selected. The resulting impedance, which is too small, is supplemented to 124 Ω with resistors R 2 and R 4 and to 150 Ω with R 3 and R 5.

The resulting slight level loss is corrected by the computer which adjusts the amplifier output voltage accordingly.

The capacitors C 2 and C 4 and C 3 and C 5 connected parallel to these additional resistors have the task of slightly increasing the output level at the upper end of the frequency band. In addition, the increased resonance of the series-tuned circuit formed by the transformer and the parallel capacitors is utilized to provide emphasis at the upper end of the frequency band:

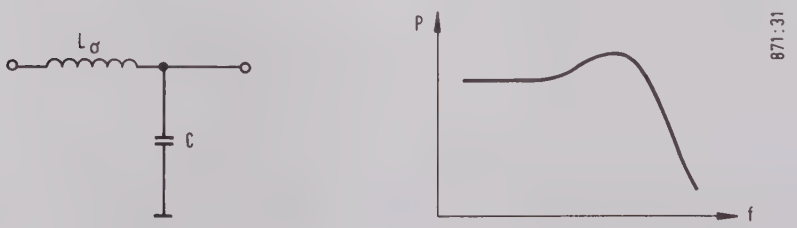


Figure 9-15 Emphasis of frequency response at upper end of band

An increase of the level at low frequencies is achieved with capacitor C 1 and the main inductance and operates as described above:

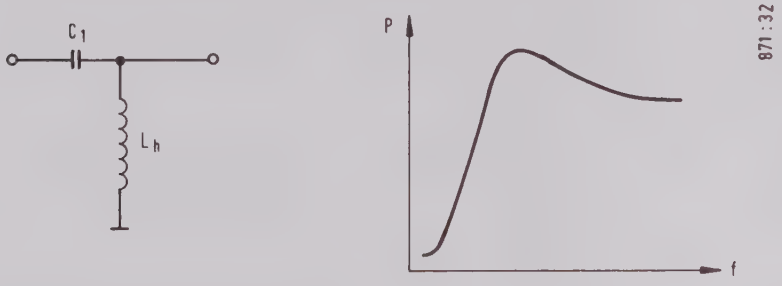


Figure 9-16 Emphasis at lower end of frequency band

The impedance of the transformer together with the source impedence of the amplifier forms a voltage divider, whose ratio varies from circuit to circuit. This variation is cancelled out by adjusting the division ratio with R 1 and P 1 to a constant value. The resulting transmission loss, which is always the same, is taken into account and corrected, together with the other losses, by the computer program when the level is set.

9.2.10.3 Board "output amplifier"

The output amplifier consists essentially of three amplifier stages, a negative feedback loop and an offset regulation:
(See block diagram of amplifier)

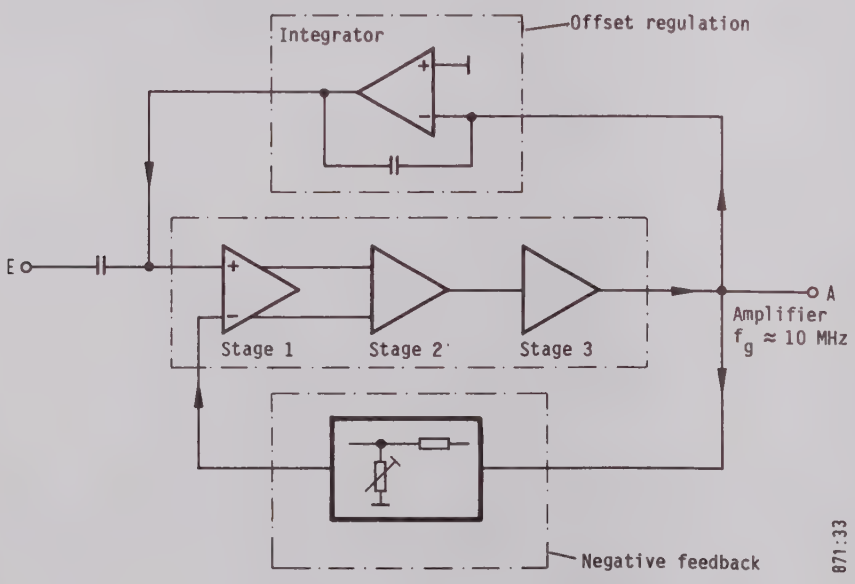


Figure 9-17 Block diagram of output amplifier

The first stage with T 1, T 2 and T 3 is a differential amplifier with a gain of 20 dB. The following current push-pull stage with T 5 and T 6 provides a further voltage gain of 40 dB. The last stage consists of IC 1. This contains an emitter-coupled complementary push-pull output stage in order to provide the necessary load current (current gain approximately 30 dB). The voltage gain of this circuit is approximately 0 dB. The resistors R 34, R 36 limit the current in the case of a short circuit; for thermal reasons, the amplifier output cannot withstand a permanent short circuit (not longer than approximately 1 minute).

A passive negative feedback path over the whole set of amplifier stages is used for gain adjustment and frequency response compensation. The resistors R 40, R 41 and the trimmer P 2 are used for adjusting the voltage for the "0 dB" gain. The resistors R 40, R 42, R 43 and trimmer P 3 are used for the "10 dB" adjustment.

However, the actual gain is approximately 0.5 dB and approximately 10.5 dB, respectively.

C 32 and L 1 and C 36/C 37 are used for correction of the frequency response at the upper limit frequency.

In order to prevent biasing of the following transformer 0 2 by direct current, IC 2 regulates the DC offset of the output amplifier to zero volts.

9.2.10.4 Board "output 3"

The transformer on board "output 3" balances the output of the "Z_{out} = 0" amplifier and is matched to the impedances Z_{out} = 150/600 Ω with the appropriate resistors R 141, R 142, R 143, R 144.

The capacitors C 41, C 43, C 44, C 45 are used for frequency response correction at the upper frequency limit. C 41 corrects the frequency response in the case Z_{in} = 0, Z_{out} = 150 Ω.

C 46 provides additional balancing of the transformer, and spaces provided on the board for a further capacitor for adjustment (C 47).

9.2.10.5 Board "relay driver"

The board "relay driver" receives the control signals and the supply voltages via a 14-pole flat cable from the CPU motherboard.

As the control signals are too weak, they must be amplified. This is carried out with one transistor per control signal. The only exception to this is relay 6, which can be energized only if relay 1 is also energized. Diode Gl 16 raises the common emitter potential to ensure that transistors which are not activated by control signals remain in the off condition.

MP MASTER
MA33540

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